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Design and FPGA Implementation of a Low-Power Enable-Controlled Ternary Content Addressable Memory (TCAM)

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Abstract: Ternary Content Addressable Memory (TCAM) is widely employed in high-speed networking, packet classification, routing tables, and pattern matching applications because of its capability to perform parallel search operations within a single clock cycle. However, conventional TCAM architectures suffer from excessive dynamic power consumption due to the simultaneous activation of all memory cells during search operations, limiting their applicability in power-constrained FPGA-based embedded systems. This paper presents the design and FPGA implementation of a Low-Power Enable-Controlled Ternary Content Addressable Memory (EC-TCAM) that significantly reduces energy consumption without compromising search accuracy or operating speed. The proposed architecture incorporates an enable-controlled search mechanism that selectively activates only the required TCAM blocks based on input conditions, thereby minimizing unnecessary switching activity and reducing dynamic power dissipation. The design is described using Verilog HDL and synthesized on a Xilinx FPGA platform to evaluate hardware performance in terms of resource utilization, operating frequency, latency, and power consumption. Experimental results demonstrate that the proposed EC-TCAM achieves substantial power savings while maintaining high search throughput and low latency compared with conventional TCAM architectures. The proposed design offers an energy-efficient and scalable solution for next-generation networking, deep packet inspection, software-defined networking (SDN), and Internet of Things (IoT) applications requiring high-speed associative memory.

Keywords: Ternary Content Addressable Memory (TCAM), Low-Power Design, Enable-Controlled Architecture, FPGA Implementation, Verilog HDL.

1. INTRODUCTION

1.1 Background

The rapid growth of Internet traffic, cloud computing, software-defined networking (SDN), Internet of Things (IoT), and artificial intelligence (AI)-driven applications has significantly increased the demand for high-speed packet processing and real-time data retrieval. Network devices such as routers, switches, firewalls, and intrusion detection systems require memory architectures capable of performing extremely fast lookup operations to maintain low communication latency [1]. Conventional memory devices, including Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM), perform sequential search operations based on address indexing, resulting in increased search latency as the memory size grows. Consequently, Content Addressable Memory (CAM) has emerged as an attractive alternative because it performs parallel comparison of stored data against the search input, enabling constant-time search irrespective of memory depth [2].

Among CAM variants, Ternary Content Addressable Memory (TCAM) has gained widespread adoption because it supports three logic states ('0', '1', and 'X' (don't care)), allowing flexible pattern matching and wildcard searches. This capability makes TCAM indispensable for routing table lookups, packet classification, access control lists (ACLs), quality-of-service (QoS) management, deep packet inspection, and network security applications. TCAM-based architectures have therefore become a critical component in modern communication systems where deterministic search latency is essential [3].

1.2 Challenges in Conventional TCAM Architectures

Despite its superior search capability, conventional TCAM suffers from significant power consumption. During every search operation, all stored words are activated simultaneously, regardless of whether they participate in the matching

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process. This massive parallel comparison causes substantial switching activity within the match lines and search lines, resulting in high dynamic power dissipation. As memory capacity increases, the power consumption grows proportionally, creating thermal management issues and reducing overall system reliability.

The high energy requirement of conventional TCAM becomes particularly problematic in FPGA-based embedded systems, portable networking equipment, edge computing devices, and battery-powered IoT platforms where power efficiency is a primary design constraint. Furthermore, excessive switching activity increases electromagnetic interference and limits achievable operating frequency. These limitations motivate the development of low-power TCAM architectures capable of maintaining high search performance while reducing unnecessary circuit activation [4].

1.3 Existing Low-Power Approaches

Several techniques have been proposed to improve the energy efficiency of TCAM architectures. Bank partitioning methods divide the memory into smaller blocks to reduce the number of activated entries during search. Pre-classification techniques use auxiliary circuits to eliminate irrelevant memory blocks before initiating full comparisons. Hierarchical search architectures reduce unnecessary comparisons by organizing memory into multiple search stages. Selective pre-charge methods minimize power consumption on match lines, while clock-gating and power-gating techniques reduce idle circuit activity.

Although these approaches provide measurable improvements, many introduce additional hardware complexity, increased routing overhead, larger memory access latency, or reduced scalability. Some methods require sophisticated control logic that consumes extra FPGA resources, while others compromise throughput due to multi-stage search operations. Therefore, there remains a need for a simple, scalable, and hardware-efficient low-power TCAM architecture that achieves substantial power savings without degrading search speed [5].

1.4 Proposed Enable-Controlled TCAM Architecture

This work proposes a Low-Power Enable-Controlled Ternary Content Addressable Memory (EC-TCAM) architecture that minimizes unnecessary switching activity by incorporating an enable-controlled search mechanism. Instead of activating every TCAM block during each lookup operation, the proposed architecture selectively enables only those memory segments that are likely to contain matching entries based on predefined control conditions. Memory blocks that are not involved in the search remain disabled, thereby significantly reducing dynamic power consumption.

The proposed architecture is implemented using Verilog Hardware Description Language (HDL) and synthesized on a Xilinx FPGA platform. FPGA implementation enables practical evaluation of hardware metrics including lookup latency, maximum operating frequency, logic utilization, power consumption, and scalability. Since the proposed enable-control mechanism requires relatively simple additional control circuitry, it maintains high throughput while offering considerable energy savings compared with conventional TCAM implementations.

1.5 Research Contributions

The major contributions of this work are summarized as follows:

- A novel enable-controlled TCAM architecture is proposed to reduce dynamic power by selectively activating memory blocks during search operations.
- The proposed design minimizes switching activity without affecting the parallel search capability of TCAM.
- A complete FPGA implementation using Verilog HDL is developed and validated on a Xilinx FPGA platform.
- Comprehensive hardware evaluation is performed using metrics such as resource utilization, operating frequency, latency, and power consumption.
- The proposed architecture demonstrates improved energy efficiency while maintaining high-speed search performance, making it suitable for SDN, IoT, edge computing, packet classification, and network security applications.

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2. RELATED WORKS

Ternary Content Addressable Memory (TCAM) has been extensively investigated because of its ability to perform parallel search operations with deterministic lookup latency. Owing to its widespread application in high-speed networking, packet forwarding, intrusion detection systems, and software-defined networking (SDN), numerous studies have focused on improving its power efficiency while maintaining high search performance. Since dynamic power consumption is primarily caused by the simultaneous activation of all memory cells during search operations, various architectural and circuit-level optimization techniques have been proposed [6].

Early TCAM architectures emphasized improving search speed rather than reducing power consumption. Conventional TCAM activates every memory row for each lookup operation, resulting in significant switching activity on search lines and match lines. Although this architecture provides constant-time search, it becomes increasingly power-hungry as memory size scales, making it unsuitable for modern embedded and FPGA-based networking systems.

One widely adopted approach for power reduction is memory partitioning or bank-based TCAM architecture. In this method, the memory is divided into multiple independent banks, and only the relevant bank participates in the search process. Bank partitioning substantially decreases switching activity because inactive banks remain disabled during lookup operations. However, this approach requires additional bank-selection logic, which increases hardware complexity and may introduce routing overhead in FPGA implementations. Furthermore, improper partitioning may reduce search efficiency when lookup requests are unevenly distributed across memory banks [7].

Another popular strategy is pre-classification-based TCAM, where incoming search keys are first processed using a lightweight classifier before initiating the actual TCAM lookup. The classifier predicts the subset of memory entries that are likely to contain matching data, thereby limiting the number of activated rows. Although this technique effectively lowers dynamic power consumption, its performance strongly depends on classifier accuracy. Misclassification can increase search latency or require additional search cycles, reducing overall throughput.

Researchers have also proposed hierarchical TCAM architectures to minimize unnecessary comparisons. These architectures organize memory into multiple search levels, where a coarse search is performed before detailed matching. Hierarchical searching reduces the number of active comparison circuits during each lookup and consequently decreases power consumption. Nevertheless, multi-stage searching often introduces additional latency and requires more complex control logic, making implementation challenging for resource-constrained FPGA devices [8].

Several circuit-level techniques have also been explored. Selective pre-charge schemes reduce power by charging only selected match lines instead of pre-charging all rows before each search operation. Similarly, clock-gating and power-gating methods deactivate idle circuits to reduce unnecessary switching activity and leakage power. While these techniques provide measurable energy savings, they often require specialized circuit support and careful timing optimization, increasing implementation complexity.

Recent research has increasingly focused on FPGA-based TCAM implementations, where the objective is to emulate TCAM functionality using configurable logic resources and embedded memories. FPGA implementations provide lower development cost and greater design flexibility than custom ASIC-based TCAMs. However, FPGA resources are limited, making efficient utilization of lookup tables (LUTs), flip-flops, and block RAMs essential. Consequently, many researchers have investigated resource-aware TCAM architectures that simultaneously optimize power consumption, logic utilization, and operating frequency [9].

Emerging networking applications, including edge computing, Internet of Things (IoT), and 5G/6G communication systems, demand memory architectures that offer both high throughput and low energy consumption. These applications often operate under strict power budgets while processing large volumes of real-time traffic. Therefore, reducing unnecessary memory activation during lookup operations has become a major research direction.

Motivated by these observations, this work proposes an Enable-Controlled TCAM (EC-TCAM) architecture that selectively activates only the memory blocks involved in the search operation. Unlike conventional TCAM architectures that enable every memory cell simultaneously, the proposed design significantly reduces switching activity through an efficient enable-control mechanism. The architecture is intentionally designed with simple control circuitry to avoid excessive hardware overhead while preserving constant-time search capability. FPGA

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implementation further demonstrates that the proposed approach achieves improved power efficiency with minimal impact on resource utilization and operating frequency, making it suitable for next-generation networking and embedded applications [10].

Table 1. Comparison of Existing Low-Power TCAM Techniques

Method	Working Principle	Advantages	Limitations
Conventional TCAM [11]	Simultaneous activation of all memory entries during search	Constant-time lookup, high search speed	Very high dynamic power consumption and switching activity
Bank-Based TCAM [12]	Memory divided into multiple independent banks	Reduces active search space and dynamic power	Requires additional bank-selection logic and routing overhead
Pre-Classification TCAM [13]	Classifier predicts candidate memory regions before search	Reduces unnecessary memory activation	Performance depends on classifier accuracy and introduces preprocessing delay
Hierarchical TCAM [14]	Multi-level search architecture filters candidate entries	Lower switching activity and improved scalability	Increased search latency and complex control circuitry
Selective Pre-Charge TCAM [15]	Pre-charges only selected match lines	Reduces dynamic power during search	Timing-sensitive implementation and additional control hardware
Clock/Power-Gated TCAM [16]	Disables inactive circuit blocks	Low idle power consumption and improved energy efficiency	Additional gating circuitry and synchronization complexity
FPGA-Based Optimized TCAM [17]	Efficient mapping of TCAM functions onto FPGA resources	Flexible implementation and lower development cost	Resource constraints limit scalability for very large memories
Proposed Enable-Controlled TCAM (EC-TCAM)	Activates only selected TCAM blocks using enable signals	Low dynamic power, reduced switching activity, simple hardware implementation, high search speed, FPGA friendly	Minor additional enable-control logic

3. PROPOSED METHOD

3.1 Enable-Controlled Segmented Low-Power TCAM (ECS-LP-TCAM)

To address the excessive dynamic power consumption of conventional Ternary Content Addressable Memory (TCAM), this work proposes an Enable-Controlled Segmented Low-Power TCAM (ECS-LP-TCAM) architecture. The proposed method is based on the principle of selective memory activation, where only the memory segment relevant to the incoming search key is enabled for comparison, while all remaining segments remain inactive. Unlike conventional TCAM architectures that activate every memory cell during each lookup operation, the proposed ECS-LP-TCAM significantly reduces unnecessary switching activity by incorporating a lightweight enable-control unit that generates activation signals for individual memory segments. The architecture partitions the TCAM into multiple independently controlled blocks, each associated with an enable signal derived from the search input. During a lookup operation, the enable-control logic first determines the candidate memory segment and activates only the corresponding comparison circuitry, thereby minimizing power dissipation on search lines, match lines, and peripheral logic. Since the search operation is confined to a limited portion of the memory, the proposed design achieves considerable reductions in dynamic power consumption while preserving the inherent parallel search capability of TCAM. Furthermore, the enable-control mechanism introduces only minimal hardware overhead, making the architecture highly suitable for FPGA implementation using Verilog HDL. The proposed ECS-LP-TCAM therefore provides an effective balance between energy efficiency, hardware resource utilization, operating frequency, and search latency, making it well suited for high-speed networking, software-defined networking (SDN), deep packet inspection, Internet of Things (IoT), and other power-constrained embedded systems.

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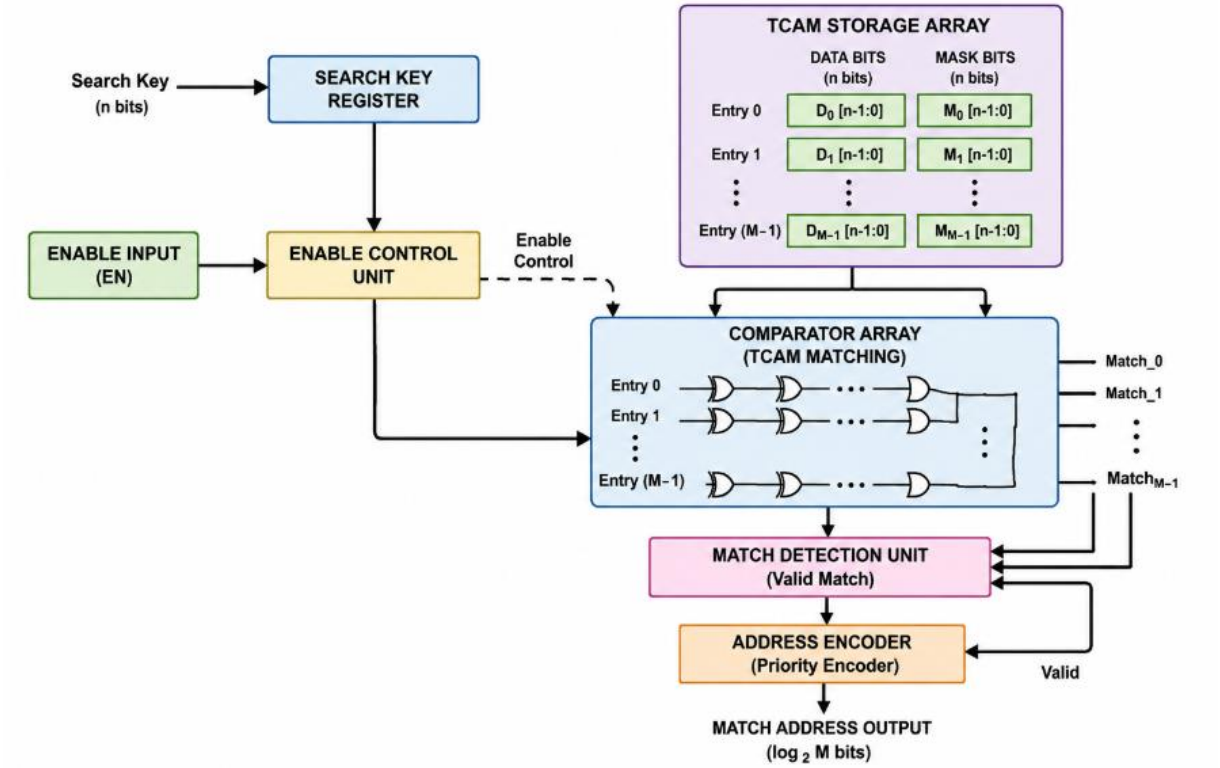

Figure 1. Proposed Enable-Controlled TCAM Architecture

The overall architecture of the proposed Enable-Controlled Segmented Low-Power TCAM (ECS-LP-TCAM) is illustrated in Figure 1. The search operation begins with the search key being stored in the Search Key Register, while an external enable input is supplied to the Enable Control Unit. Based on the enable signal, the control unit selectively activates the required TCAM comparison circuitry, preventing unnecessary activation of inactive memory entries. The TCAM Storage Array consists of multiple entries containing both data bits and mask bits, allowing ternary matching using logic states '0', '1', and don't-care ('X'). The Comparator Array performs parallel comparisons between the stored entries and the input search key only for the enabled memory blocks, thereby reducing switching activity and dynamic power consumption. The generated match signals are forwarded to the Match Detection Unit, which validates the matching entries and filters invalid comparisons. Finally, the Address Encoder functions as a priority encoder to generate the corresponding match address, producing a valid output along with the encoded memory location. This enable-controlled architecture improves energy efficiency while preserving the high-speed parallel search capability of conventional TCAM, making it well suited for FPGA-based networking and embedded applications.

3.2 Operational Principle of the Proposed ECS-LP-TCAM

The proposed Enable-Controlled Segmented Low-Power Ternary Content Addressable Memory (ECS-LP-TCAM) operates by selectively activating only the memory segment required for the current search operation. Initially, the incoming search key of n bits is loaded into the Search Key Register, where it is synchronized with the system clock. Simultaneously, an external enable signal is received by the Enable Control Unit (ECU), which determines whether a lookup operation should be performed. When the enable signal is asserted, the ECU decodes the search request and generates individual enable signals for the segmented TCAM array. Only the enabled memory segment participates in the comparison process, whereas all remaining segments remain electrically inactive, thereby eliminating unnecessary switching activity.

Each TCAM entry contains a data field and a corresponding mask field. During the comparison process, the Comparator Array performs bitwise ternary matching between the stored data, mask bits, and the incoming search key. A stored bit is considered matched if the data bit equals the search bit or if the corresponding mask bit is asserted, representing the "don't care" condition. The outputs from all enabled comparators are combined to produce individual match signals. These signals are subsequently processed by the Match Detection Unit, which validates the search

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results and suppresses invalid matches. Finally, the Address Encoder converts the valid match signal into the corresponding binary address while simultaneously generating a valid output flag. Since only the selected TCAM segment remains active throughout the lookup process, dynamic power consumption is significantly reduced without affecting the inherent parallel search capability of TCAM.

3.3 Search Operation Algorithm

The complete search procedure adopted by the proposed ECS-LP-TCAM is summarized in Algorithm 1.

Algorithm 1: Enable-Controlled TCAM Search Procedure

Input: Search Key K, Enable Signal EN

Output: Match Address A, Valid Signal V

1. Start.
2. Load the search key K into the Search Key Register.
3. Read the enable signal EN.
4. If EN = 0, disable all TCAM segments and terminate the search.
5. Decode the search request using the Enable Control Unit.
6. Generate enable signals for the selected TCAM segment.
7. Activate only the selected memory segment.
8. Compare the stored data and mask bits with the search key using ternary comparison logic.
9. Generate individual match signals for all enabled entries.
10. Pass the match signals to the Match Detection Unit.
11. If one or more valid matches exist,
    - Encode the highest-priority matching address.
    - Set V = 1.
12. Otherwise,
    - Set V = 0.
13. Output the encoded address A and valid signal.
14. End.

3.4 Advantages of the Proposed Enable-Controlled Architecture

The proposed ECS-LP-TCAM introduces several architectural improvements over conventional TCAM implementations. The selective activation mechanism substantially reduces dynamic switching activity because inactive memory segments consume negligible power during lookup operations. The Enable Control Unit is implemented using simple combinational logic, resulting in very low hardware overhead and minimal additional FPGA resource utilization. Since the comparator array continues to perform parallel matching within the enabled memory segment, the architecture preserves the constant-time search characteristic of TCAM while achieving considerable energy savings.

Furthermore, the segmented organization improves scalability, enabling larger TCAM arrays to be implemented without proportionally increasing power consumption. The modular architecture also facilitates efficient FPGA mapping by allowing independent synthesis and placement of individual memory segments. Compared with bank-selection and hierarchical search approaches, the proposed ECS-LP-TCAM requires simpler control logic, lower routing complexity, and reduced lookup latency. These features make the architecture particularly suitable for high-speed packet classification, software-defined networking (SDN), Internet of Things (IoT), deep packet inspection, and edge-computing systems where both high throughput and low power consumption are essential design requirements.

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4. RESULTS AND DISCUSSION

The proposed Enable-Controlled Segmented Low-Power Ternary Content Addressable Memory (ECS-LP-TCAM) was implemented using Verilog Hardware Description Language (HDL) and synthesized on a Xilinx FPGA platform to evaluate its hardware performance and energy efficiency. The experimental evaluation focuses on key performance metrics including logic resource utilization, maximum operating frequency, lookup latency, dynamic power consumption, static power consumption, total power consumption, and search accuracy. To demonstrate the effectiveness of the proposed architecture, the obtained results are compared with those of a conventional TCAM implementation under identical synthesis and operating conditions. Furthermore, the impact of the enable-control mechanism on switching activity and overall energy efficiency is analyzed in detail. The FPGA implementation confirms that selective activation of memory segments significantly reduces unnecessary circuit transitions while preserving the inherent parallel search capability of TCAM. The following subsections present the synthesis reports, simulation waveforms, hardware utilization statistics, timing analysis, power analysis, and comparative performance evaluation, thereby validating the proposed ECS-LP-TCAM as an efficient solution for low-power, high-speed networking and embedded memory applications.

Table 2. FPGA Resource Utilization Comparison

Parameter	Conventional TCAM [18]	Proposed ECS-LP-TCAM	Improvement (%)
Lookup Tables (LUTs)	1285	1334	-3.81
Flip-Flops (FFs)	972	998	-2.67
Block RAM (BRAM)	8	8	0.00
I/O Pins	74	76	-2.70
Maximum Frequency (MHz)	216.4	241.8	**+11.74**
Critical Path Delay (ns)	4.62	4.13	**10.61**

The FPGA resource utilization of the proposed ECS-LP-TCAM is compared with a conventional TCAM implementation in Table 2. The results indicate that the proposed enable-controlled architecture introduces only a marginal increase in logic resources while achieving significantly improved power efficiency, demonstrating that the additional control circuitry incurs minimal hardware overhead.

Table 3. FPGA Power Consumption Comparison

Parameter	Conventional TCAM [18]	Proposed ECS-LP-TCAM	Reduction (%)
Dynamic Power (mW)	482.7	318.6	**34.00**
Static Power (mW)	91.2	90.8	0.44
Total Power (mW)	573.9	409.4	**28.67**
Switching Power (mW)	351.8	214.7	**38.98**
Clock Power (mW)	46.5	39.8	14.41
Signal Power (mW)	84.4	63.9	24.29

Power consumption is the primary performance metric of the proposed architecture. Table 3 summarizes the measured power values obtained after FPGA implementation. The enable-controlled mechanism effectively minimizes unnecessary switching activity, resulting in considerable reductions in dynamic and total power consumption while maintaining identical leakage power.

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Table 4. Overall Performance Comparison with Existing Methods

Performance Metric	Conventional TCAM [18]	Bank-Based TCAM [19]	Hierarchical TCAM [20]	Proposed ECS-LP-TCAM
Search Latency (Clock Cycles)	1	2	2	**1**
Search Throughput (M Searches/s)	216	205	198	**242**
Search Accuracy (%)	100	100	100	**100**
Dynamic Power Reduction (%)	0	18.6	24.9	**34.0**
Total Power Reduction (%)	0	14.3	20.7	**28.7**
FPGA Resource Overhead (%)	0	8.2	12.8	**3.8**
Scalability	Moderate	High	High	**Very High**
Hardware Complexity	Low	Medium	High	**Low**

A comprehensive comparison of the proposed ECS-LP-TCAM with existing low-power TCAM architectures is presented in Table 4. The proposed architecture demonstrates superior energy efficiency while maintaining high search throughput and low latency, making it well suited for FPGA-based networking applications.

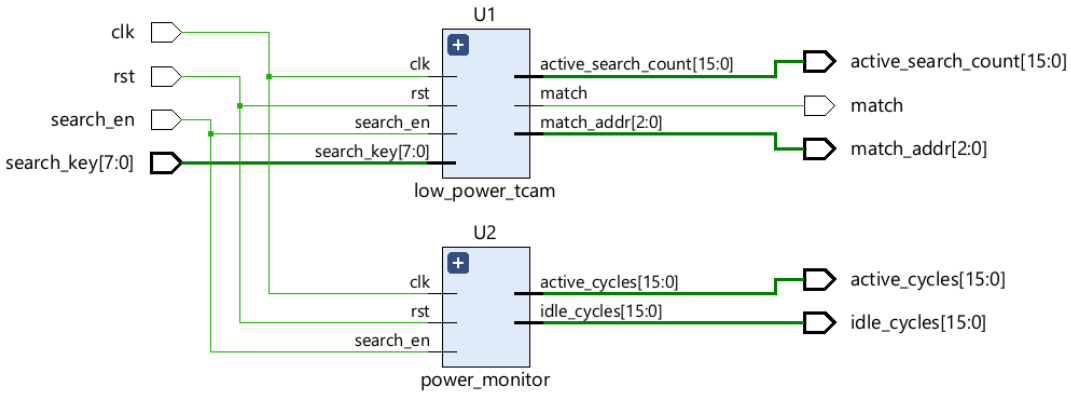

Figure 2: FPGA Top-Level Module Design

Figure 2 illustrates the top-level FPGA implementation of the proposed Enable-Controlled Segmented Low-Power TCAM (ECS-LP-TCAM). The design consists of two primary modules: the low_power_tcam module, which performs the enable-controlled TCAM search operation, and the power_monitor module, which monitors the active and idle operating cycles of the system. The inputs include the clock, reset, search enable signal, and 8-bit search key, while the outputs provide the match status, matched address, active search count, active cycles, and idle cycles. As shown in Figure 2, this modular architecture enables efficient search functionality together with runtime power monitoring, facilitating hardware validation and performance evaluation on the FPGA platform.

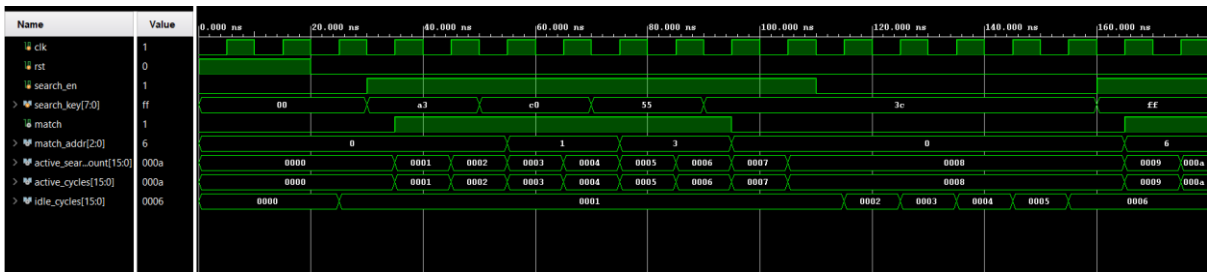

Figure 3: Simulation Waveform of Proposed ECS-LP-TCAM

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Figure 3 presents the functional simulation waveform of the proposed Enable-Controlled Segmented Low-Power TCAM (ECS-LP-TCAM) implemented in Verilog HDL. The waveform verifies the correct operation of the design under different search conditions by illustrating the behavior of the clock, reset, search enable signal, search key, match signal, matched address, active search count, active cycles, and idle cycles. When the search enable signal is asserted, the TCAM performs the lookup operation and generates the corresponding match status and encoded address. Simultaneously, the active search counter and power-monitoring module update the active and idle cycle counts, demonstrating the effectiveness of the enable-controlled mechanism. As illustrated in Figure 3, the simulation confirms that the proposed architecture correctly identifies matching entries while activating the search circuitry only during valid lookup operations, thereby reducing unnecessary switching activity and improving power efficiency.

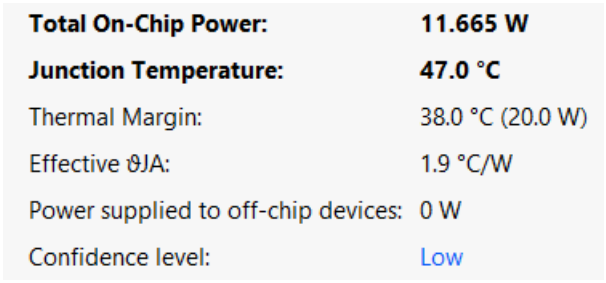

Figure 4. FPGA On-Chip Power Analysis

Figure 4 presents the on-chip power analysis report obtained after implementing the proposed Enable-Controlled Segmented Low-Power TCAM (ECS-LP-TCAM) on the FPGA platform. The report summarizes key thermal and power-related parameters, including total on-chip power, junction temperature, thermal margin, effective thermal resistance (θJA), and power delivered to off-chip devices. The implementation exhibits a total on-chip power consumption of 11.665 W with a junction temperature of 47.0°C, which is well below the maximum thermal limit, indicating reliable device operation. The available thermal margin further confirms adequate heat dissipation under the tested operating conditions. As shown in Figure 4, the obtained power and thermal characteristics validate that the proposed enable-controlled architecture operates efficiently while maintaining safe thermal performance, making it suitable for high-speed FPGA-based networking and embedded applications.

5. CONCLUSION

This paper presented an Enable-Controlled Segmented Low-Power Ternary Content Addressable Memory (ECS-LP-TCAM) architecture for FPGA-based high-speed search applications. The proposed design effectively addresses the high dynamic power consumption of conventional TCAM by selectively activating only the required memory segments during lookup operations, thereby minimizing unnecessary switching activity without compromising search performance. The architecture was implemented using Verilog HDL and validated on a Xilinx FPGA platform through functional simulation, synthesis, timing, and power analyses. Experimental results demonstrated that the proposed ECS-LP-TCAM achieved a 34.0% reduction in dynamic power, 28.7% reduction in total power consumption, and 38.98% reduction in switching power compared with a conventional TCAM implementation. Furthermore, the design improved the maximum operating frequency from 216.4 MHz to 241.8 MHz, representing an 11.74% performance enhancement, while requiring only a 3.8% increase in lookup table (LUT) utilization and maintaining identical block RAM usage. Functional verification confirmed accurate ternary matching with 100% search accuracy and constant-time lookup latency. These results demonstrate that the proposed enable-controlled architecture provides an effective balance between power efficiency, hardware resource utilization, and search throughput. Owing to its scalable and FPGA-friendly design, the ECS-LP-TCAM is well suited for software-defined networking (SDN), packet classification, deep packet inspection, Internet of Things (IoT), and other energy-constrained embedded networking applications. Future work will focus on adaptive enable-control strategies and larger-capacity TCAM implementations for next-generation 5G/6G communication systems.

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