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Design and Implementation of a Digital Coherence BFSK Demodulator Using FPGA

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Abstract

In this paper, we propose the design and implementation mechanism for a digital coherence BFSK demodulator based on the use of Direct Digital Frequency Synthesizer (DDFS) and digital filter using Cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1. The proposed demodulator has the following parameters**:**

-Clock frequency: F_{CLK}=50MHz.

-Sampling frequency : f_{sam}= 40 KHz : (f_{sam}= F_{CLK}/ K=50000 KHz /1250 =40 KHz).

-Cut-off frequency of the digital low pass filters (LPF-1, LPF-2) is f_{cut1} = f_{cut2} =0.450 KHz.

-Modulation type of signal is: BFSK .

-The data signal is square pulse with frequency : F_{data}= 0.100 KHz .

-Carrier type: is sinusoidal with frequency: f_{car0}=1.2 KHz , f_{car1}=2.1 KHz.

-The ROM capacity for the stored signal samples (8192X8) bits, and their values are positive within the range from 0 to 255.

-Frequency range: (3 Hz…25 MHz).

-Frequency Resolution: (3 Hz).

- Signal amplitude (5V).

-Using FPGA allows for the modification and development of the digital design to suit the designer's wishes and goals.

Keywords: digital demodulator , BFSK , DDFS , FPGA, LPF

I. INTRODUCTION

1- The BFSK signal is given according to the following mathematical relation [1]:

$$V(t)_{BFSK(0)} = A.cos(w_{car0}t) \quad for \ \ bit \ 0 \qquad (1)$$

$$V(t)_{BFSK(1)} = A.cos(w_{car1}t) \quad for \ \ bit \ 1 \qquad (2)$$

Where :

$w_{car0}=2\pi f_{car0}$, $w_{car1}=2\pi f_{car1}$ carrier frequencies , $w_{data}=2\pi f_{data}$ data signal frequency and (A) amplitude of the BFSK signal.

2-The carrier signal is given according to the following mathematical relation:

$$V(t)_{car0} = cos(w_{car0}t) = cos(2\pi f_{car0}t) \qquad (3)$$

$$V(t)_{car1} = cos(w_{car1}t) = \cos(2\pi f_{car1}t) \qquad (4)$$

For transmitted bit 0

3-The signal of the product carrier signal and BFSK signal in channel (0) is given according to the following mathematical relation:

$$V_0 = V(t)_{BFSK(0)}\, V(t)_{car0} = \{A.cos(w_{car0}t)\} * \{cos(w_{car0}t)\} \qquad (5)$$

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$$V_0 = V(t)_{BFSK(0)} V(t)_{car0} = \frac{A}{2}\{cos(0) + \cos(2w_{car0}t)\} \quad (6)$$

$$V_0 = V(t)_{BFSK(0)}\, V(t)_{car0} = \frac{A}{2} + \frac{A}{2}\cos(2w_{car0}t) \quad (7)$$

4- The output signal of the digital low pass filter (LPF-1):

$$y_0 = \frac{A}{2} \quad (8)$$

5-The signal of the product carrier signal and BFSK signal in channel (1) is given according to the following mathematical relation:

$$V_1 = \ V(t)_{BFSK(0)}\, V(t)_{car1} = \{A.cos(w_{car0}t)\} * \{cos(w_{car1}t)\} \quad (9)$$

$$V_1 = V(t)_{BFSK(0)} V(t)_{car1} = \frac{A}{2}[cos\{(w_{car0} + w_{car1})t\} + cos\{(w_{car0} - w_{car1})t\}] \quad (10)$$

$$V_1 = V(t)_{BFSK(0)}\, V(t)_{car1} = \frac{A}{2}cos\{(w_{car0} + w_{car1})t\} + \frac{A}{2}cos\{(w_{car0} - w_{car1})t\} \quad (11)$$

6- The output signal of the digital low pass filter (LPF-2):

$$y_1 = 0 \quad (12)$$

For transmitted bit 1

1-The signal of the product carrier signal and BFSK signal in channel (0) is given according to the following mathematical relation:

$$V_0 = \ V(t)_{BFSK(1)}\, V(t)_{car0} = \{A.cos(w_{car1}t)\} * \{cos(w_{car0}t)\} \quad (13)$$

$$V_0 = V(t)_{BFSK(1)} V(t)_{car0} = \frac{A}{2}[cos\{(w_{car1} + w_{car0})t\} + cos\{(w_{car1} - w_{car0})t\}] \quad (14)$$

$$V_0 = V(t)_{BFSK(1)}\, V(t)_{car1} = \frac{A}{2}cos\{(w_{car1} + w_{car0})t\} + \frac{A}{2}cos\{(w_{car1} - w_{car0})t\} \quad (15)$$

2- The output signal of the digital low pass filter (LPF-1):

$$y_0 = 0 \quad (16)$$

3-The signal of the product carrier signal and BFSK signal in channel (1) is given according to the following mathematical relation:

$$V_1 = \ V(t)_{BFSK(1)}\, V(t)_{car1} = \{A.cos(w_{car1}t)\} * \{cos(w_{car1}t)\} \quad (17)$$

$$V_1 = V(t)_{BFSK(1)} V(t)_{car1} = \frac{A}{2}cos(0) + \frac{A}{2}cos(2w_{car1}t) \quad (18)$$

$$V_1 = V(t)_{BFSK(1)} V(t)_{car1} = \frac{A}{2} + \frac{A}{2}cos(2w_{car1}t) \quad (19)$$

4- The output signal of the digital low pass filter (LPF-2):

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$$y_1 = \frac{A}{2} \qquad (20)$$

Decision Rule

$$\begin{Bmatrix} \text{If } y_0 > y_1 \implies received\ bit = 0 \\ \text{If } y_1 > y_0 \implies received\ bit = 1 \end{Bmatrix} \qquad (21)$$

The block diagram of the digital coherence BFSK demodulator using DDFS and digital filter is shown in the figure (1).

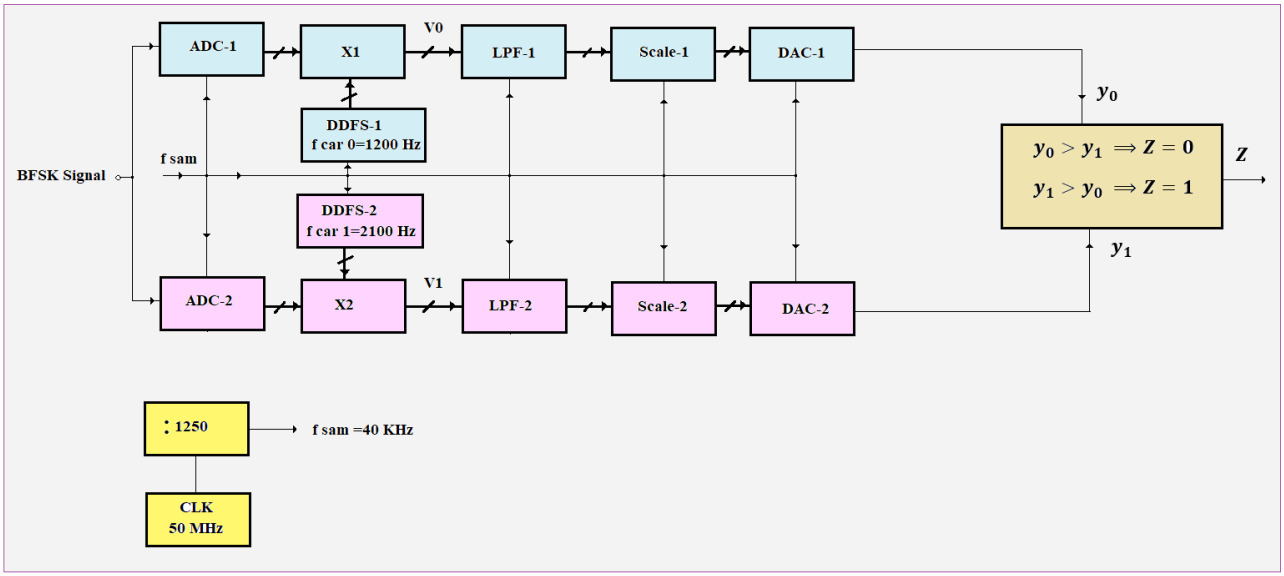

Fig. 1: The block diagram of the digital coherence BFSK demodulator using the DDFS and a digital filters.

Previous studies have explored various approaches for reliable BFSK detection. Some researchers relied on PLL- based carrier recovery circuits to achieve synchronization [2], which introduced system complexity, increased sensitivity to noise, and required settling time. Alternatively, other researchers adopted non-coherent detection [3] to completely avoid phase issues, but at the expense of degraded performance and higher bit error rates for the same signal-to-noise ratio. This work presents an innovative solution that overcomes these limitations by using two shared DDFS generators between the transmitter and receiver, achieving complete frequency and phase synchronization without the need for complex circuitry, while maintaining high performance and consuming fewer resources compared to both previous approaches.

II. RESERCH IMPORTANCE AND ITS OBJECTIVES

-In this paper, a digital coherence BFSK demodulator was designed, implemented and tested based on the use of - Digital Direct Frequency Synthesizer (DDFS) using FPGA , VHDL and Graphical programming language with Quartus II 9.1 design environment.

-Using the digital DDFS with mathematical operations (adding , multiply , division ,filtering) , makes the digital demodulation design process flexible, accurate and highly efficient.

-Changing the parameters of data signal (frequency and amplitude), carrier frequency explains the difference between digital demodulation and analog demodulation.

III. RESERCH MATERIALS AND ITS WAYS

To design, and test the digital demodulator for different modulation types of signals, the following tools and software are used:

-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [4].

-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.

-VHDL programming language with Quartus II 9.1 design environment [5].

-Design Environment MATLAB R2008a

-GDS-1052 digital oscilloscope with Free Wave program to take the results.

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-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [6] is shown in figure (2).

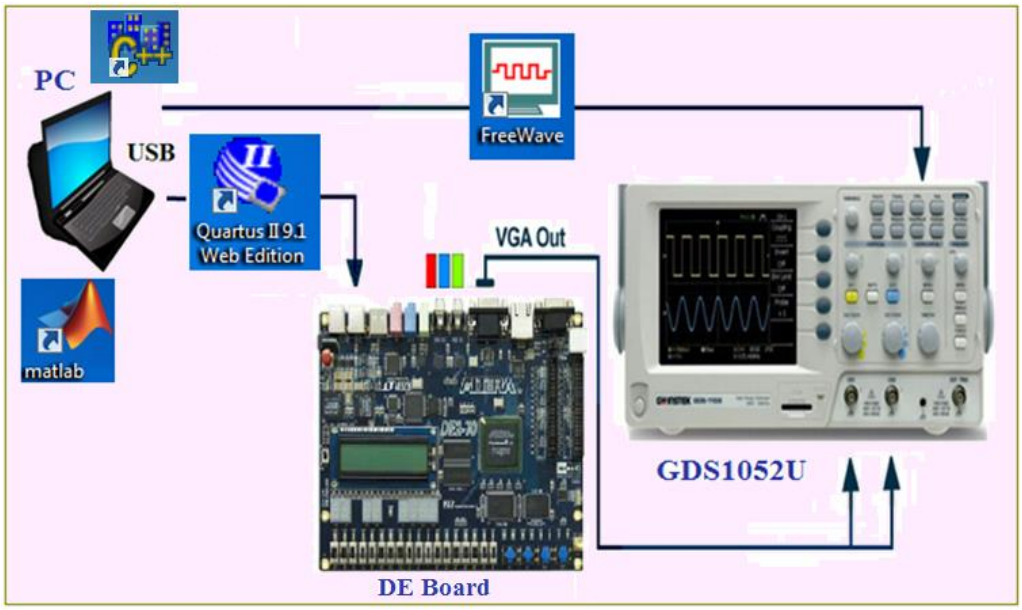

Fig (2): Block diagram of the laboratory experiment platform

IV. THE DESIGN STAGES OF THE DIGITAL BFSK DEMODULATOR WITH USB USING THE DDFS

For transmitted bit 0

1-Convert the analog BFSK signal to digital signal using ADC , where :

$$f_{sam} >= 2\,(f_{car1} + F_{data})$$

For samples of BFSK signals [7] :

$$V_{BFSK(0)}(T_{sam}.n) = A\,.\,cos(2\pi.T_{sam}.n.f_{car0}) = A.cos\left(\frac{2\pi.n.f_{car0}}{f_{sam}}\right) \qquad (22)$$

2-Formation the samples of a carrier signals using DDFS according to the mathematical relationship.

$$V_{car0}(T_{sam}.n) = \cos\,(2\pi f_{car0}.n\,.T_{sam}) = cos\left(\frac{2\pi\ .n\,.f_{car0}}{f_{sam}}\right) \qquad (23)$$

$$V_{car1}(T_{sam}.n) = cos\,(2\pi f_{car1}.n\,.T_{sam}) = cos\left(\frac{2\pi\ .n\,.f_{car1}}{f_{sam}}\right) \qquad (24)$$

3-Formation of the product signal between samples of BFSK signal and carrier signal samples using DDFS.

$$V_0 = V_{BFSK(0)}(T_{sam}.n).V_{car0}(T_{sam}.n)$$

$$V_0 = A.cos\left(\frac{2\pi.n.f_{car0}}{f_{sam}}\right).cos\left(\frac{2\pi\,.n\,.f_{car0}}{f_{sam}}\right) \qquad (25)$$

$$V_0 = \frac{A}{2}.cos\left(\frac{4\pi.n.f_{car0}}{f_{sam}}\right) + \frac{A}{2}.\cos(0) = \frac{A}{2}.cos\left(\frac{4\pi.n.f_{car0}}{f_{sam}}\right) + \frac{A}{2}$$

4-The following component are removed using a digital low pass filter (LPF-1):

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$$\frac{A}{2} cos\left(\frac{4\pi.n.f_{car0}}{f_{sam}}\right) \quad (26)$$

5- The output signal of the low pass filter (LPF-1):

$$y_0 = V(n)_{dem1} = \frac{A}{2} \quad (27)$$

6-In the same way ,we obtain the following:

$$V_1 = V_{BFSK(0)}(T_{sam}.n).V_{car1}(T_{sam}.n)$$

$$V_1 = A.cos\left(\frac{2\pi.n.f_{car0}}{f_{sam}}\right).cos\left(\frac{2\pi.n.f_{car1}}{f_{sam}}\right) \quad (28)$$

$$V_1 = \frac{A}{2}.cos\left\{\frac{2\pi.n.(f_{car1}+f_{car0})}{f_{sam}}\right\} + \frac{A}{2}.cos\left\{\frac{2\pi.n.(f_{car1}-f_{car0})}{f_{sam}}\right\}$$

$$y_1 = V(n)_{dem2} = 0 \quad (29)$$

$$y_0 > y_1 \Longrightarrow Z = 0 \quad (30)$$

For transmitted bit 1

1-Convert the analog BFSK signal to digital signal using ADC , where :

$$f_{sam} >= 2\ (f_{car1} + F_{data})$$

For samples of BFSK signals [7] :

$$V_{BFSK(1)}(T_{sam}.n) = A.cos(2\pi.T_{sam}.n.f_{car1}) = A.cos\left(\frac{2\pi.n.f_{car1}}{f_{sam}}\right) \quad (31)$$

2-Formation of the product signal between samples of BFSK signal and carrier signal samples using DDFS.

$$V_0 = V_{BFSK(1)}(T_{sam}.n).V_{car0}(T_{sam}.n)$$

$$V_0 = A.cos\left(\frac{2\pi.n.f_{car1}}{f_{sam}}\right).cos\left(\frac{2\pi.n.f_{car0}}{f_{sam}}\right) \quad (32)$$

$$V_0 = \frac{A}{2}.cos\left\{\frac{2\pi.n.(f_{car1}+f_{car0})}{f_{sam}}\right\} + \frac{A}{2}.cos\left\{\frac{2\pi.n.(f_{car1}-f_{car0})}{f_{sam}}\right\}$$

3- The output signal of the low pass filter (LPF-1):

$$y_0 = V(n)_{dem1} = 0 \quad (33)$$

4-In the same way ,we obtain the following:

$$V_1 = V_{BFSK(1)}(T_{sam}.n).V_{car1}(T_{sam}.n)$$

$$V_1 = A.cos\left(\frac{2\pi.n.f_{car0}}{f_{sam}}\right).cos\left(\frac{2\pi.n.f_{car1}}{f_{sam}}\right) \quad (34)$$

$$V_1 = \frac{A}{2}.cos\left(\frac{4\pi.n.f_{car0}}{f_{sam}}\right) + \frac{A}{2}.cos(0)$$

5- The output signal of the low pass filter (LPF-2):

$$y_1 = V(n)_{dem2} = \frac{A}{2} \quad (35)$$

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$$y_1 > y_0 \Longrightarrow Z = 1 \qquad (36)$$

6- Design the digital band pass filter (BPF-1 , BPF-2) using MATLB and VHDL with the following parameters [8] :

-Type of filter : LPF-1,LPF-2 .

- Filter structure : Direct form - FIR

-Filter order : 250.

-Filter length : 251.

-Sampling frequency : 40 KHz.

-Frequency of data signal : 0.100 KHz.

-Cut-off frequency of the LPF-1 , f_{cut1}=(0.450 KHz) and of LPF-2 , f_{cut2}=(0.450 KHz).

-Window type : Hamming.

-Word length : 8 bits.

The specifications and the magnitude and impulse responses of a digital filters LPF-1 and LPF-2 designed in MATLAB [9] are shown in figures (3) and (4).

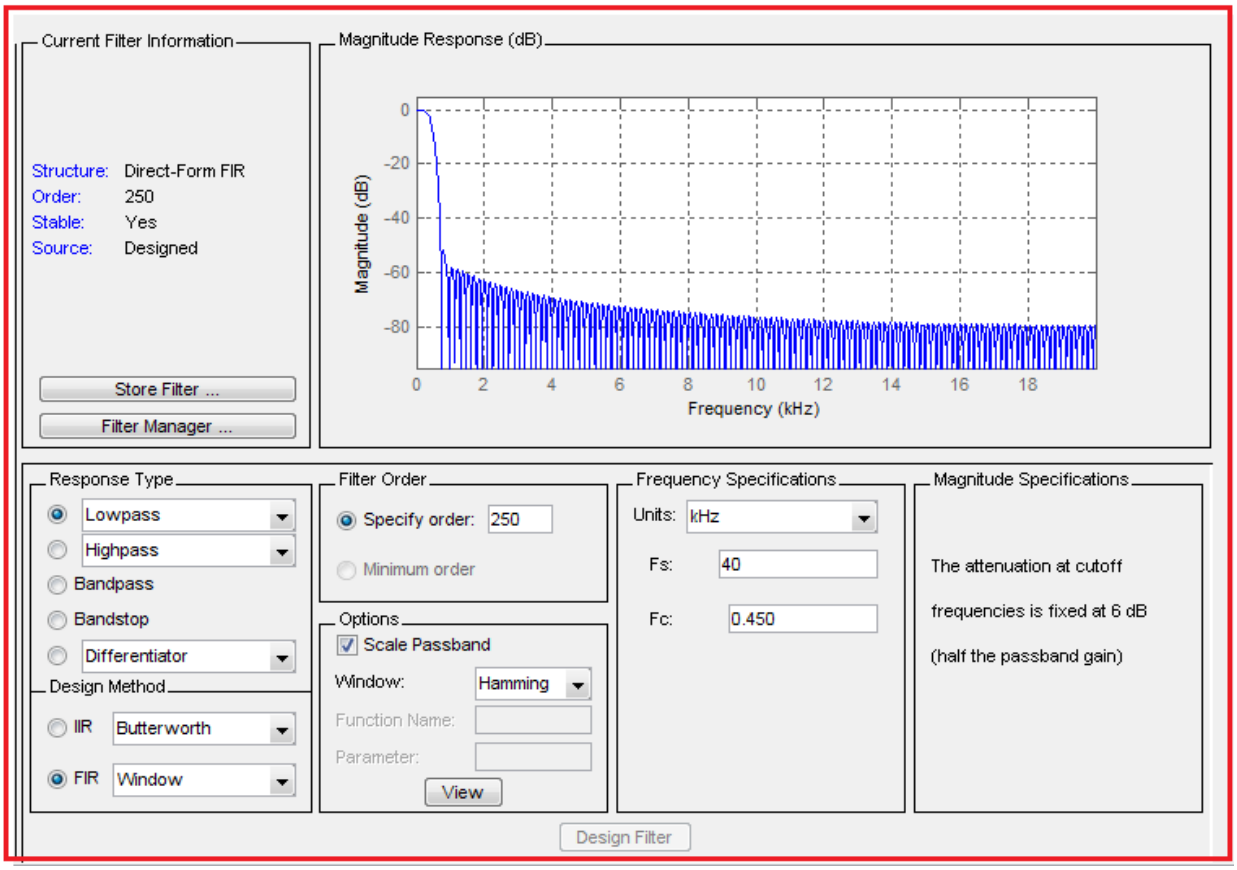

Fig (3) : The specifications and the magnitude response of a digital LPF1 designed in MATLAB.

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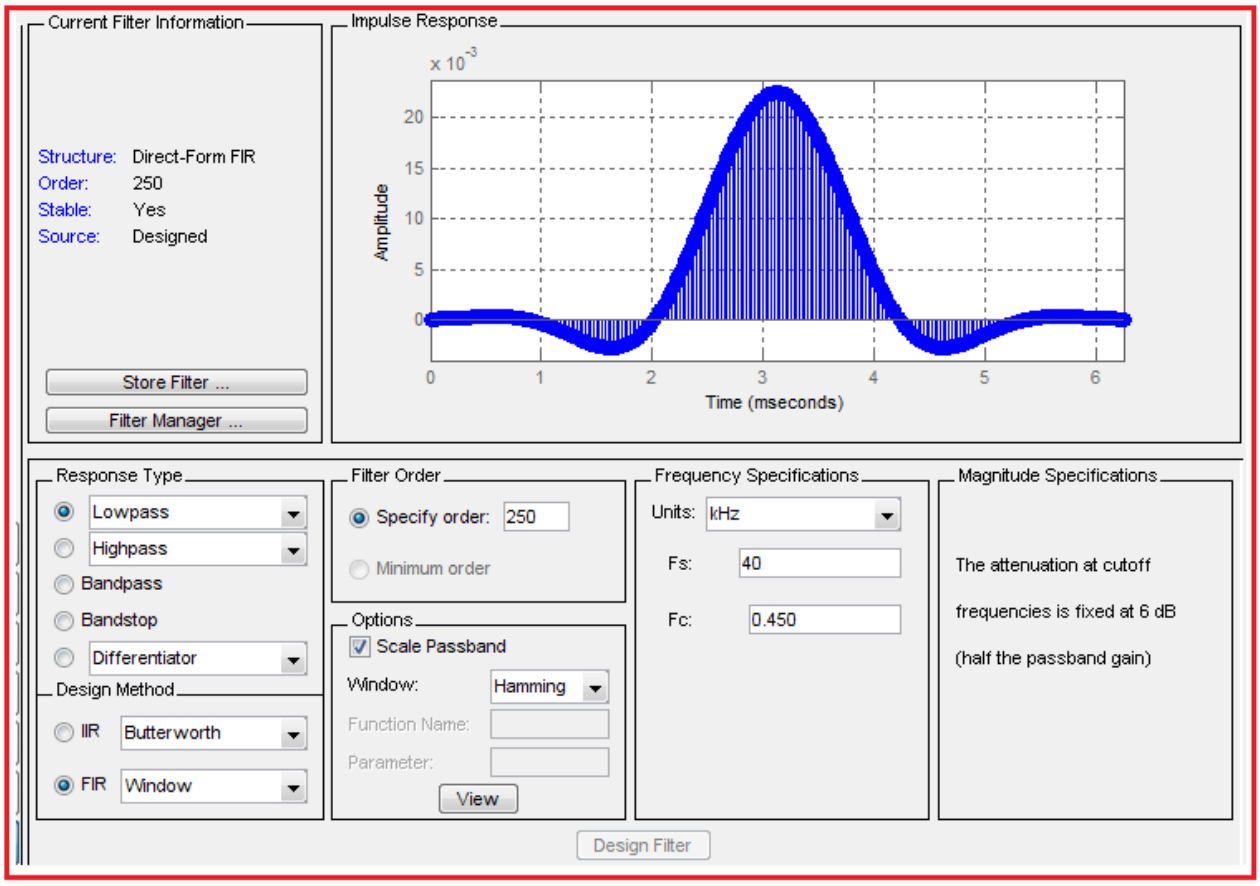

Fig (4) : The specifications and the impulse response of a digital LPF-1 and LPF-2 designed in MATLAB.

V. DESIGN OF THE DIGITAL BFSK DEMODULATOR USIGN DDFS IN QUARTUS II 9.1

We have a DDFS which has the following parameters:

-The frequency step is : $\delta f = 3\ Hz$, $F_{CLK} = 50\ MHz$.

-The data signal (data) is square pulse of frequency F_{data} =0.100 KHz and frequencies of carrier signal f_{car0}=1.2 KHz , f_{car1}=2.1 KHz.

-Modulation type: BFSK.

-The ROM capacity for the stored signal samples 8192X8 bits and their values are positive within the range from 0 to 255.

-The number of the accumulator bits is computed from the following mathematical relation [10]:

$$\delta f = \frac{F_{CLK}}{2^n} \qquad (37)$$

$$\delta f = \frac{F_{CLK}}{2^n} \Longrightarrow 2^n = \frac{F_{CLK}}{\delta f} = \frac{50\ X\ 10^6}{3} = 24 \text{ bits}$$

-The frequency range for the carrier and modulating signals synthesizer is computed from the following mathematical relation :

$$\Delta f = 0 \ldots . \frac{F_{CLK}}{2} = 0 \ldots . 25\ MHz$$

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-To synthesize four signals of frequencies $f_{sam} = 40\ KHZ$, $f_{car0} = 1.2$ KHz , $f_{car1} = 2.1$ KHz , $F_{data} = 0.100$ KHz , the frequency code must be [10]:

$$Code\ F = L = \frac{f.2^{n}}{F_{CLK}} \qquad (38)$$

$$Code\ f_{sam} = L_{sam} = \frac{f_{sam}.2^{n}}{F_{CLK}} = \frac{40\ x\ 2^{24}}{50000} = 13422$$

$$Code\ f_{car0} = L_{car0} = \frac{f_{car0}.2^{n}}{f_{sam}} = \frac{1.2\ x\ 2^{24}}{40} = 503316$$

$$Code\ f_{car1} = L_{car1} = \frac{f_{car1}.2^{n}}{f_{sam}} = \frac{2.1\ x\ 2^{24}}{40} = 880804$$

$$Code\ F_{data} = L_{data} = \frac{F_{data}.2^{n}}{f_{sam}} = \frac{0.100x\ 2^{24}}{40} = 41943$$

The functional diagram of a digital amplitude BFSK modulator and coherence digital BFSK demodulator in Quartus II 9.I design environment is shown in figure (5), it consists of :

-BFSK-DDFS is allocated for shaping a digital coherence BFSK signal.

-CAR-DDFS is allocated for shaping a digital carrier signal with frequency 1.2 KHz and 2.1KHz

-DATA-GEN is allocated for shaping a square pulse signal with frequency 0.100 KHz.

-DEMODULATOR (digital coherence BFSK demodulator) is allocated for multiplying the BFSK signal and the carrier signal.

-LPF-1, LPF-2 (tow digital low pass filters) is allocated for a selection modulating signal.

-Sampling signal generator is allocated for shaping a square pulse with frequency 40 KHz.

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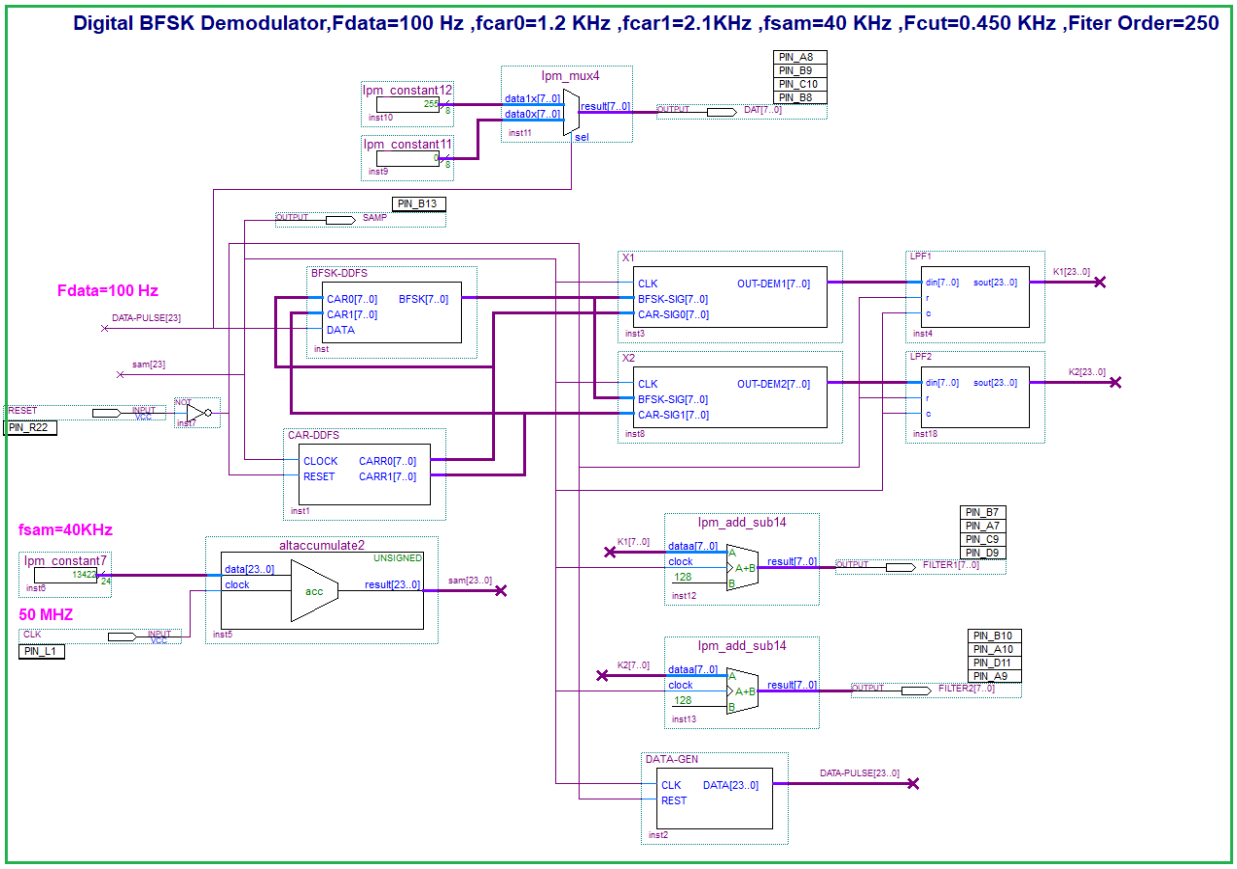

Fig (5) : The functional diagram of a digital BFSK modulator and coherence BFSK demodulator in Quartus II 9.I design environment

The block diagram of a digital BFSK- DDFS in Quartus II 9.I design environment is shown in figure (6).

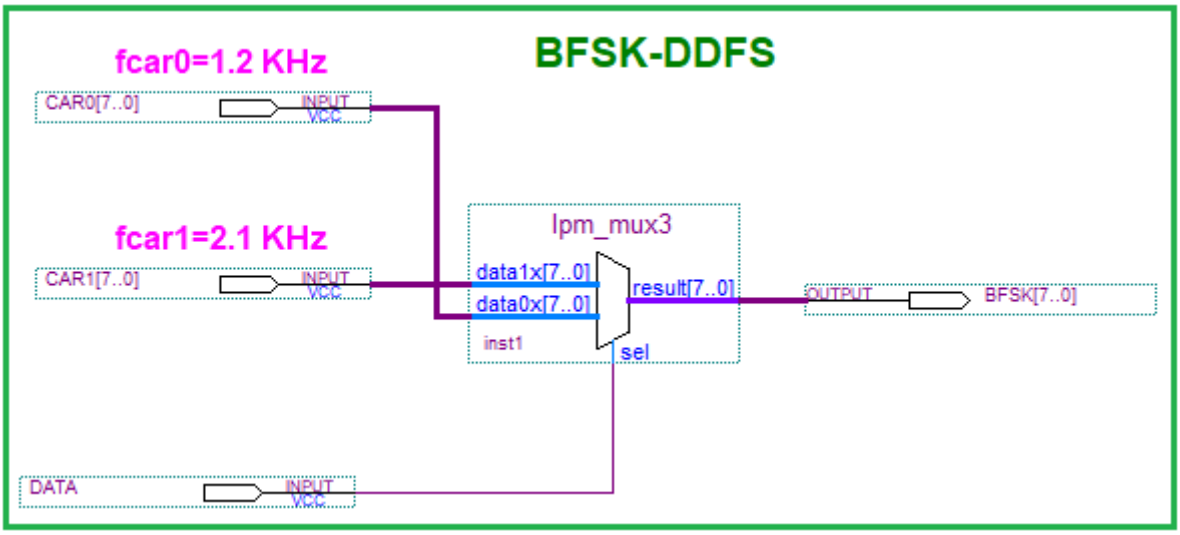

Fig (6) : The block diagram of a BFSK-DDFS in Quartus II 9.I design environment

The results of the practical design of a digital BFSK-DDFS in Quartus II 9.I design environment for f_{sam}=40 KHz and F_{data}=0.100 KHz in time domain are shown in figure (7) and in figure (8) in frequency domain .

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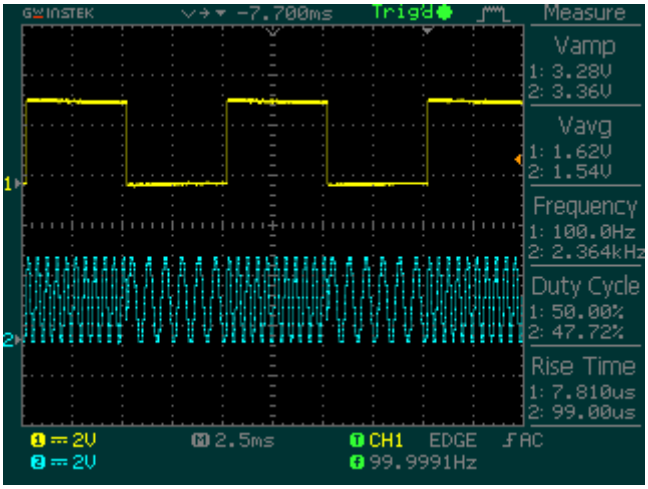

Fig. 7: The data and BFSK signals with fsam=40 KHz and F_{data}=0.100 KHz in time domain.

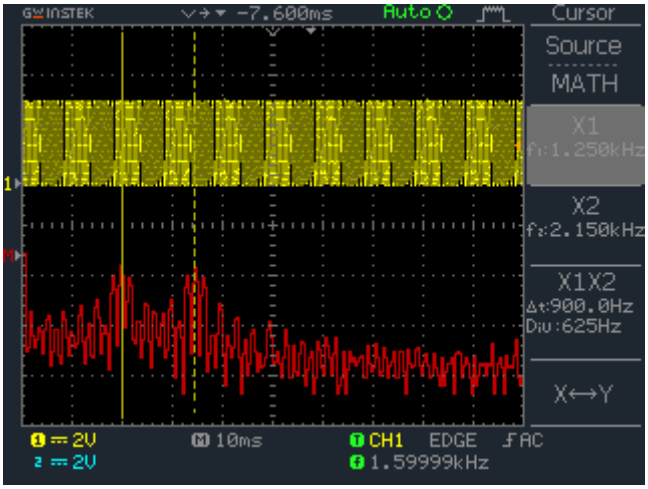

Fig. 8: The BFSK signal with fsam=40 KHz and F_{data}=0.100 KHz in frequency domain.

The block diagram of a digital carrier DDFS in Quartus II 9.I design environment is shown in figure (9).

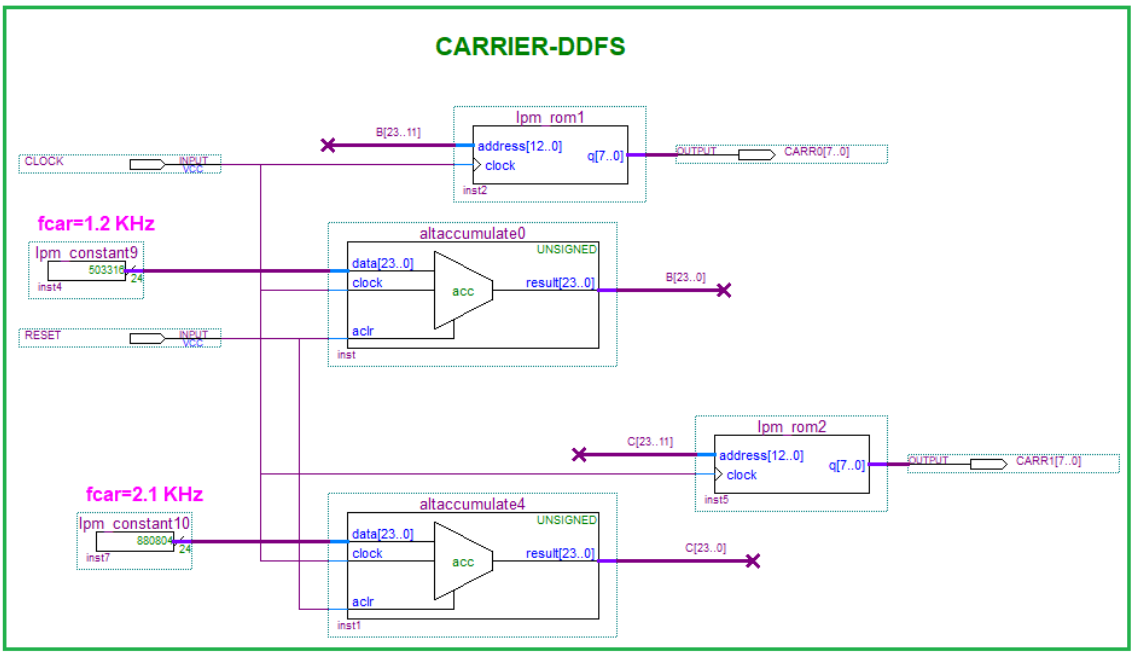

Fig (9) : The block diagram of a CARRIER-DDFS in Quartus II 9.I design environment

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The results of the practical design of a digital CARRIER-DDFS in Quartus II 9.I design environment for f_{car0}=1.2 KHz and f_{car1}=2.1 KHz in time domain are shown in figure (10) and in figure (11) in frequency domain .

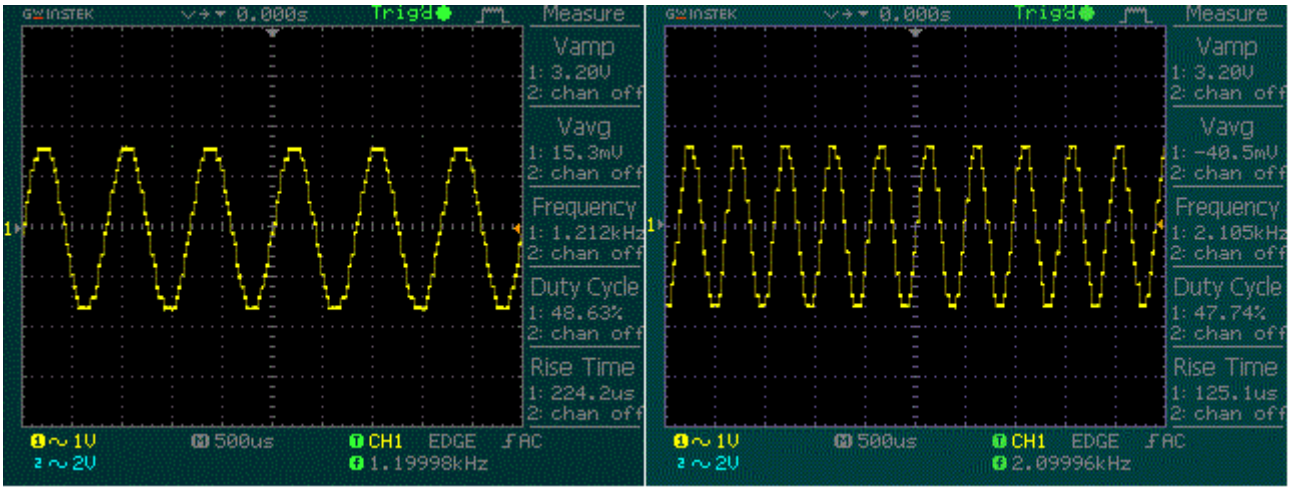

Fig. 10: The carrier0 f_{car0}=1.2 KHz and carrier1 f_{car1}=2.1 KHz signals in time domain.

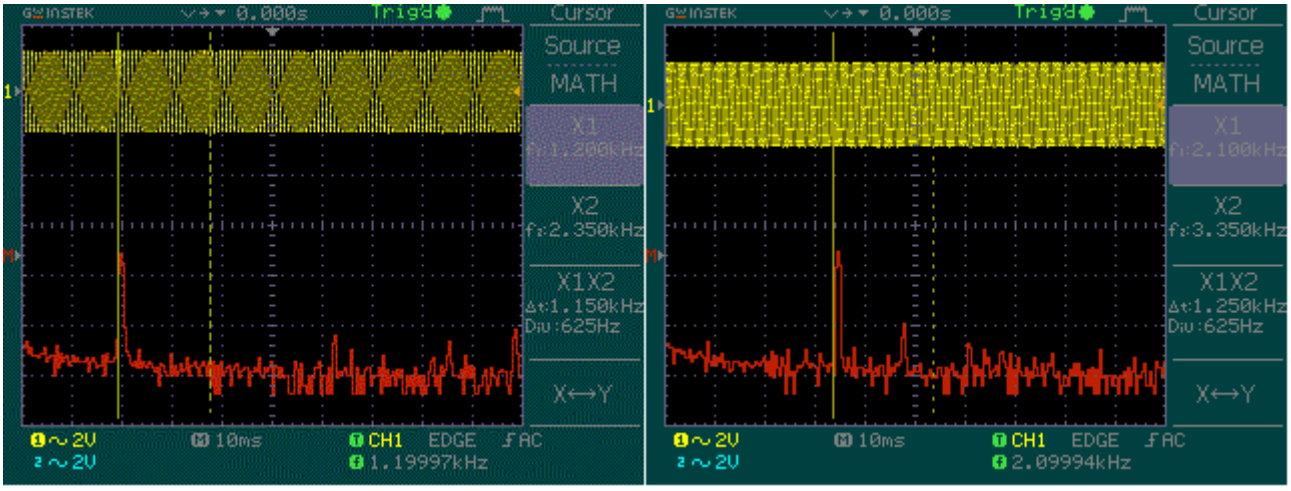

Fig. 11: The carrier0 f_{car0}=1.2 KHz and carrier1 f_{car1}=2.1 KHz signals in frequency domain.

The results of the practical design of a digital sampling generator in Quartus II 9.I design environment for for f_{sam}=40 KHz in time domain are shown in figure (12) and in figure (13) in frequency domain .

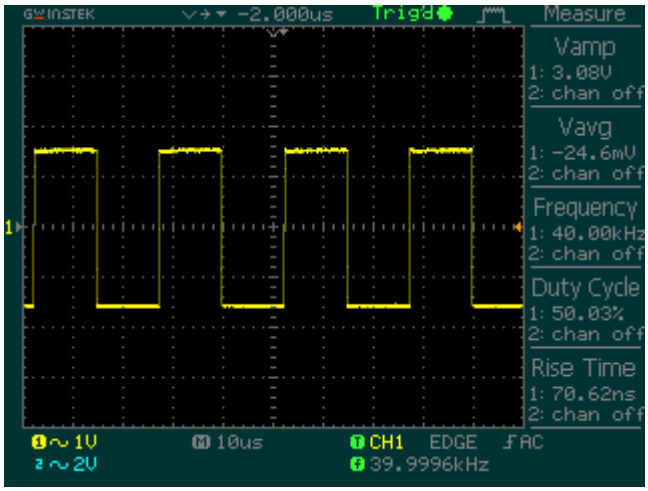

Fig. 12: The sampling signal with fsam=40 KHz in time domain.

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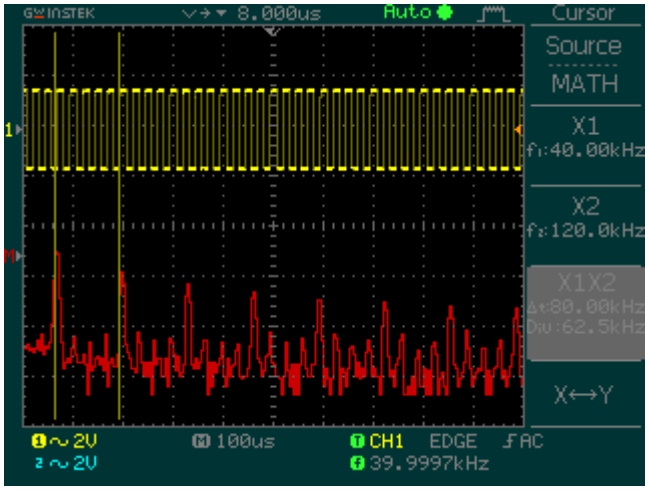

Fig. 13: The sampling with f_{sam}=40 KHz in frequency domain.

The block diagram of a digital BFSK demodulator in Quartus II 9.I design environment is shown in figure (14).

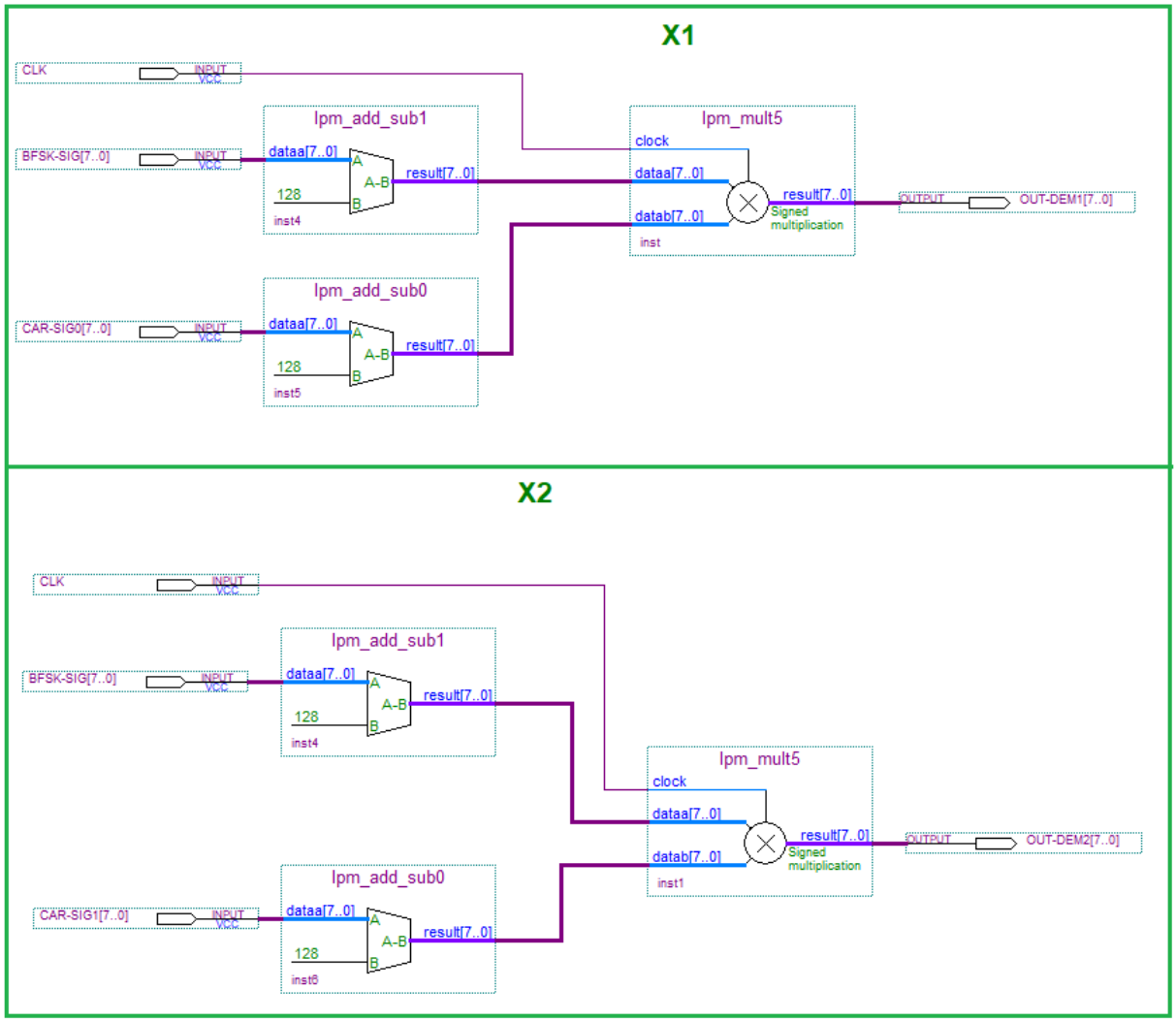

Fig (14) : The block diagram of a digital coherence BFSK demodulator in Quartus II 9.I design environment

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The block diagram of a digital data generator for F_{data}=0.100 KHz in time domain according to the previous application using the FPGA chip placed on education and development board DE1 is shown in figure. (15).

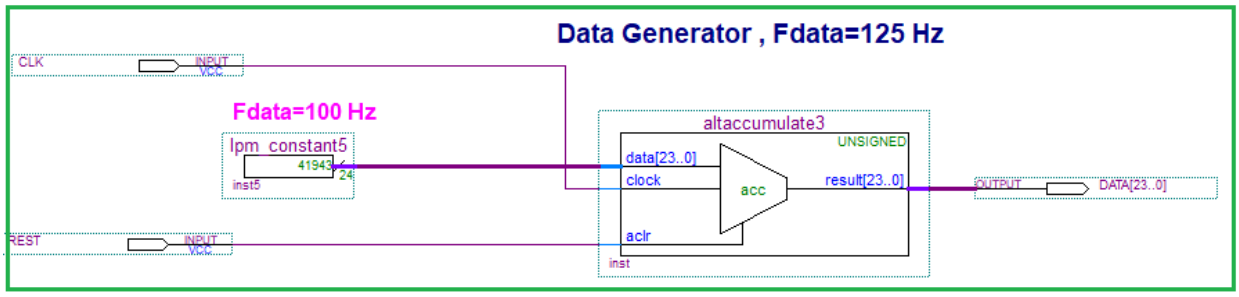

Fig (15) : The block diagram of a digital data generator in Quartus II 9.I design environment

The results of the practical design of a digital data generator for F_{data}=0.100 KHz in Quartus II 9.I design environment in time domain are shown in figure (16) and in figure (17) in frequency domain .

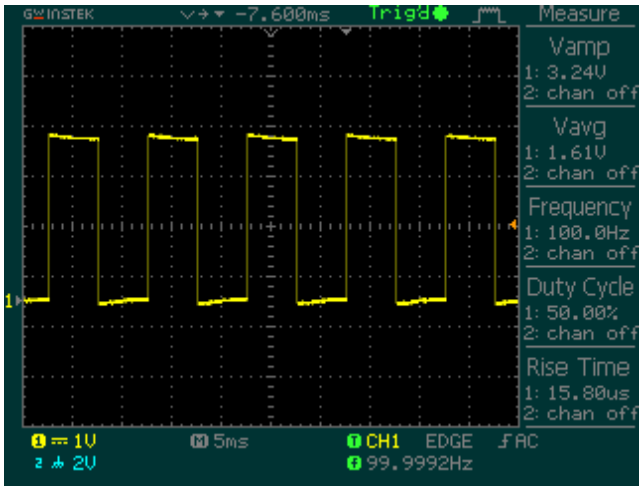

Fig. 16: The signals of digital data generator with F_{data}=0.100 KHz in time domain.

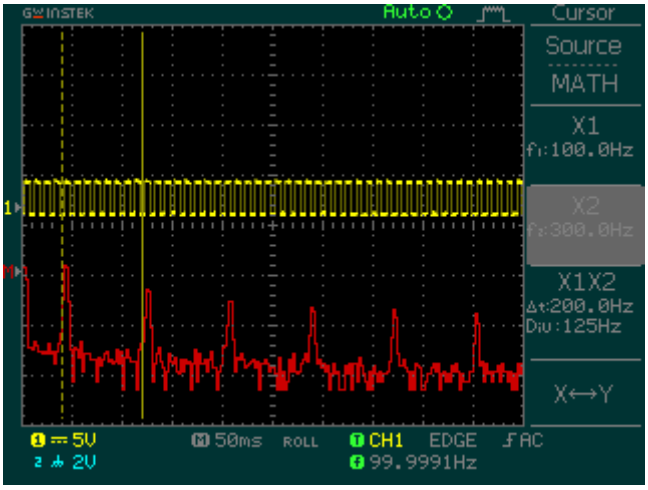

Fig. 17: The signals of digital data generator for F_{data}=0.100 KHz in frequency domain.

VI. RESULTS OF DESIGN

The results of the practical design for the digital BFSK demodulator for F_{data}=0.100 KHz, f_{car0} =1.2 KHz and f_{car1} =2.1 KHz in time domain according to the previous application using the FPGA chip placed on education and development board DE1 are shown in figure (18) for LPF-1 and in figure (19) for LPF-2.

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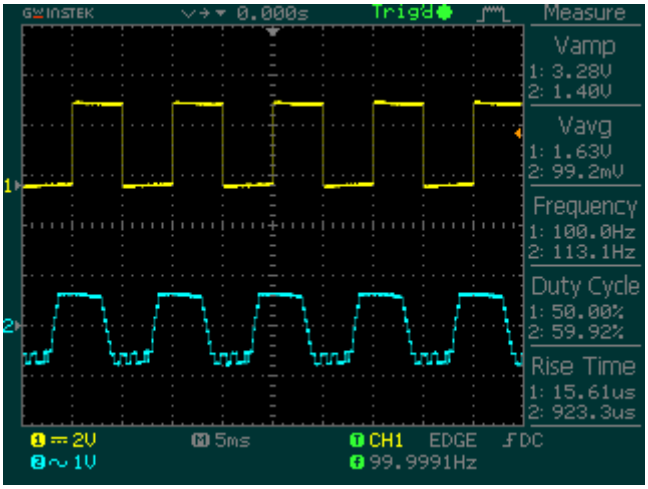

Fig. 18: The input and output data signals for LPF-1 in time domain.

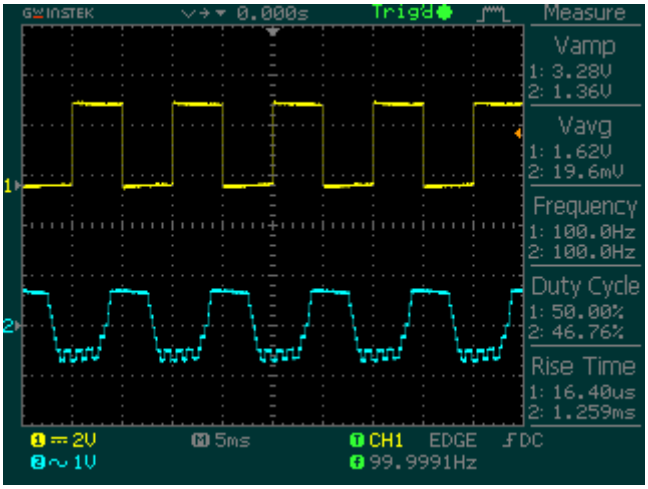

Fig. 19: The input and output data signals for LPF-2 in time domain.

The results of the practical design for the digital BFSK demodulator for F_{data}=0.100 KHz, f_{car0} =1.2 KHz and f_{car1} =2.1 KHz in time domain according to the previous application using the FPGA chip placed on education and development board DE1 are shown in figure (20) for LPF-1 and for LPF-2.

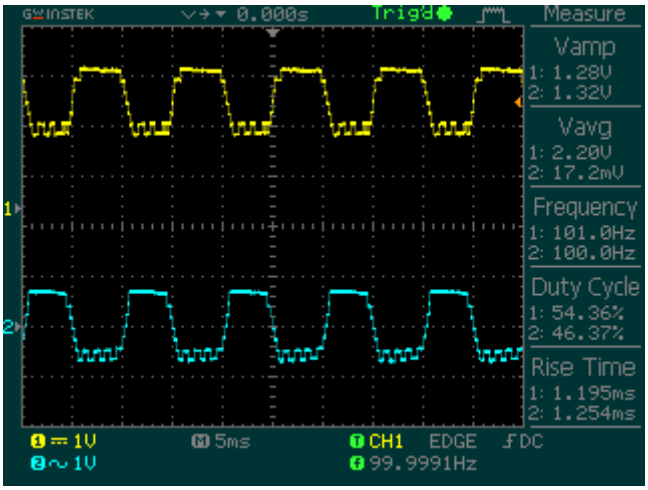

Fig. 20: The input and output data signals for LPF-1 and LPF-2 in time domain.

Figure (18) shows the original data signal (square pulses at 100 Hz) and the output signal of the first filter (LPF-1 the channel dedicate to bit '0' at 1.2 KHz).It can be observed the both signals have the same frequency, but there is a time delay between them caused by the computational processes within the 250-order filter.

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Figure (19) shows the original data signal (square pulses at 100 Hz) and the output signal of the second filter (LPF-2 the channel dedicate to bit '1' at 2.1 KHz).It can be observed the both signals have the same frequency, but there is a time delay between them caused by the computational processes within the 250-order filter.

Figure (20) combines the output signals of the first and second filters. This figure demonstrates that tow signals are perfectly time-inverted (i.e . , when one is at a high level , the other is at a low level) , which is the required behavior for proper coherent detection. This allow the data bits to be recovered simply by comparing the channels.

The results of the practical design for the digital BFSK demodulator for F_{data}=0.100 KHz, f_{car0} =1.2 KHz and f_{car1} =2.1 KHz in frequency domain according to the previous application using the FPGA chip placed on education and development board DE1 are shown in figure (21) for LPF-1.

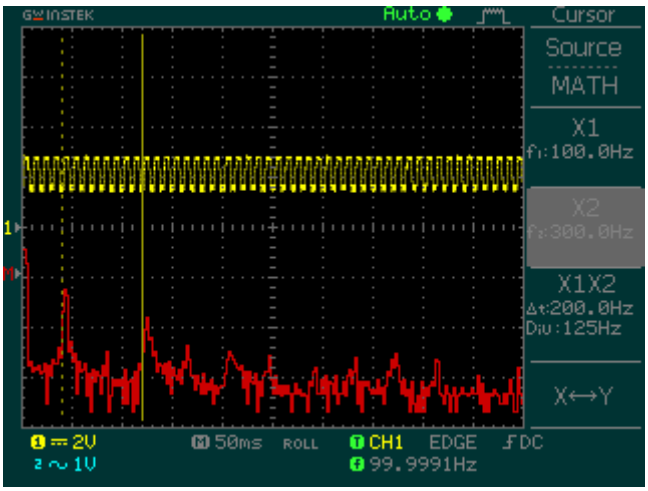

Fig. 21: The output data signal for LPF-1 in frequency domain.

These figures are taken from the screen of digital oscilloscope and digital spectrum analyzer (GDS-1052 digital oscilloscope with Free Wave program), we can notice the identification between the theoretical results and the practical results, which indicate the high accuracy of digital synthesizing and demodulation operations for these signals.

VII. DISCUSSION AND CONCLUSIONS

-Due to the significant impact of phase discontinuity in the transmitted signal on the performance of coherent detection in BFSK systems, this paper proposes and implements a design based on the use of tow independent DDFS generators to produce the tow transmitted signals (1.2 KHz for bit '0' and 2.1 KHz for bit '1').Tow identical generators are also employed in the receiver to serve as local oscillators for the tow detection channels .This arrangement insures complete frequency and phase synchronization between the received signal and the local reference ,resulting in a stable and high – performance detection process .

- Based on the practical results achieved from the implemented detector, it was found that the ripples appearing on the output signals of the LPF filters are attributed to three main factors: the small frequency difference between the bit-0 and bit-1 carriers, the low filter order due to limited FPGA resources, and the low cut-off frequency that truncates the spectrum of the modulating signal and causes distortion. Therefore, to eliminate these ripples and distortions, it is recommended to increase the frequency separation between the two carriers, raise the filter cut-off frequency, increase the filter order, and use an FPGA with larger resources.

-The use of high-order of FIR filters makes the digital filtering process of the demodulator accurate and efficient.

-The higher order of FIR , the more unwanted frequency components are removed, thus improving the demodulation process.

-Using DDFS techniques in communication domain allows implementing different digital modulation and demodulation operations with high accuracy and speed in digital signal synthesizing, and with the ability of changing parameters in wide range.

-Using DDFS techniques in communication domain allows implementing the digital processing in the communication receiver on high intermediate frequency.

-We notice from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital synthesizing and modulation operations for signals.

-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).
-The most important thing in this paper is the possibility of changing the frequency of the data generator and the frequencies of the carrier signals.

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BIOGRAPHY

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