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Design and Implementation of a Digital Coherence BPSK Demodulator using FPGA

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Abstract: JIn this paper, we propose the design and implementation mechanism for a digital coherence BPSK demodulator based on the use of Direct Digital Frequency Synthesizer (DDFS) and digital filter using Cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1. The proposed demodulator has the following parameters:

-Clock frequency: F_{CLK}=50MHz.

-Sampling frequency : f_{sam}= 40 KHz : (f_{sam}= F_{CLK}/ K=50000 KHz /1250 =40 KHz).

-Cut- off frequency of the digital low pass filter (LPF) : f_{cut}=2 KHz

-Modulation type of signal is: BPSK .

-The modulating signal is square pulse with frequency : f_{mod1}=0.25 KHz or f_{mod2}=0.125 KHz ($f_{mod1,2}$<= fcut).

-Carrier type: is sinusoidal with frequency: f_{car}=2 KHz.

-The ROM capacity for the stored signal samples (8192X8) bits, and their values are positive within the range from 0 to 255.

-Frequency range: (3 Hz…25 MHz).

-Frequency Resolution: (3 Hz).

- Signal amplitude (5V).

-Using FPGA allows for the modification and development of the digital design to suit the designer's wishes and goals.

Keywords: digital demodulator , BPSK , DDFS , FPGA

I. INTRODUCTION

1- The BPSK signal is given according to the following mathematical relation [1]:

$$V(t)_{BPSK} = A.D(t).cos(w_{car}t + \varphi_0) \quad (1)$$

Where :
$D(t) = +1 \; or \; -1$, w_{car}=2πf$_{car}$ carrier frequency , w_{mod}=2πf$_{mod}$ modulating signal frequency , (φ_0) initial phase of BPSK, (A) amplitude of the BPSK signal.
2-The carrier signal is given according to the following mathematical relation:

$$V(t)_{car} = cos(w_{car}t) = cos(2\pi f_{car}t) \quad (2)$$

3-The signal of the product carrier signal and BPSK signal is given according to the following mathematical relation:

$$V(t)_{BPSK}\, V(t)_{car} = \{A.D(t).cos(w_{car}t + \varphi_0)\} * \{V_{car}cos(w_{car}t)\} \quad (3)$$

$$V(t)_{BPSK}\, V(t)_{car} = \frac{A.D(t)}{2}\{cos(2w_{car}t + \varphi_0) + \cos(\varphi_0)\} \quad (4)$$

$$V(t)_{BPSK}\, V(t)_{car} = \frac{A.D(t)}{2}cos(2w_{car}t + \varphi_0) + \frac{A.D(t)}{2}\cos(\varphi_0) \quad (5)$$

4- Using the digital LPF with a cut-off frequency (f_{cut}) , the following signal can be removed:

$$\frac{A.D(t)}{2}cos(2w_{car}t + \varphi_0) \quad (6)$$

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5- The output signal of the digital low pass filter (LPF):

$$V(t)_{dem} = \frac{A.D(t)}{2} cos(\varphi_0) \qquad (7)$$

The block diagram of the digital coherence BPSK demodulator using DDFS and digital filter is shown in the figure (1).

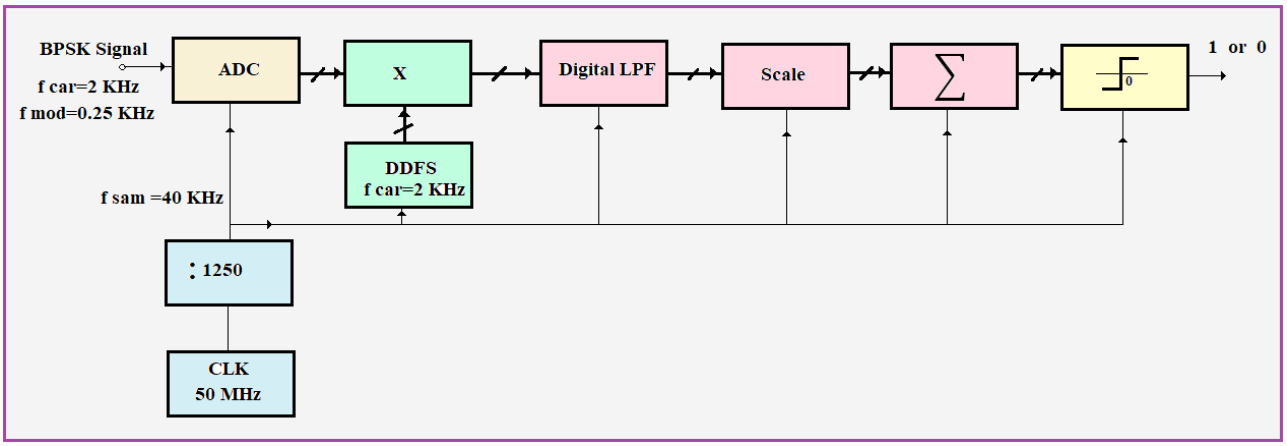

Fig. 1: The block diagram of the digital coherence BPSK demodulator using the DDFS and a digital filter.

Reference [2] presents the complex method for simulation the operation of a BPSK signal detector using NCO ,simulation and synthesis were done using Xilinx ISE12.3 Tools, this paper utilizes Quartus II 9.I design environment and VHDL programming language , and design is implemented practically.

II. RESERCH IMPORTANCE AND ITS OBJECTIVES

-In this paper, a digital coherence BPSK demodulator was designed, implemented and tested based on the use of -\ Digital Direct Frequency Synthesizer (DDFS) using FPGA , VHDL and Graphical programming language with Quartus II 9.1 design environment.
-Using the digital DDFS with mathematical operations (adding , multiply , division ,filtering) , makes the digital demodulation design process flexible, accurate and highly efficient.
-Changing the parameters of modulating signal (frequency and amplitude), carrier frequency explains the difference between digital demodulation and analog demodulation.

III. RESERCH MATERIALS AND ITS WAYS

To design, and test the digital demodulator for different modulation types of signals, the following tools and software are used:
-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].
-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment [4].
-Design Environment MATLAB R2008a
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [5] is shown in figure (2).

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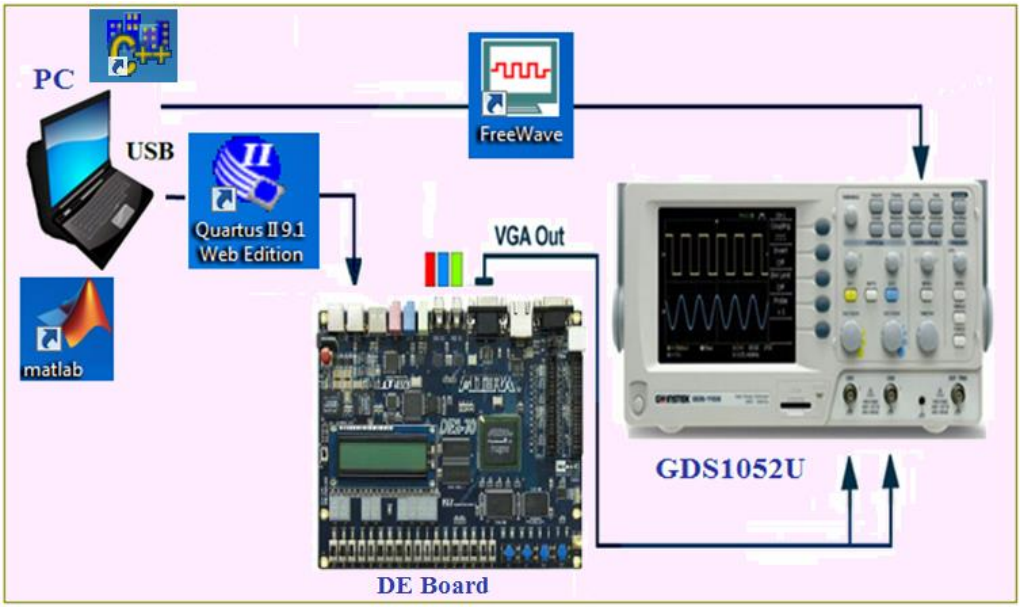

Fig (2): Block diagram of the laboratory experiment platform

IV. THE DESIGN STAGES OF THE DIGITAL BPSK DEMODULATOR WITH USB USING THE DDFS

1-Convert the analog BPSK signal to digital signal using ADC , where :

$$f_{sam}>=2\ (f_{car}+ f_{mod})$$

For samples of BPSK signal [6] :

$$V_{BPSK}(T_{sam}.n) = A\ .D(t)cos(2\pi.T_{sam}.n.f_{car} + \varphi_0) = A\ .D(t).cos\left(\frac{2\pi.n.f_{car}}{f_{sam}} + \varphi_0\right) \qquad (8)$$

2-Formation the samples of a carrier signal using DDFS according to the mathematical relationship.

$$V_{car}(T_{sam}.n) = cos\ (2\pi f_{car}.n\ .T_{sam}) = cos\left(\frac{2\pi\ .n\ .f_{car}}{f_{sam}}\right) \qquad (9)$$

3-Formation of the product signal between samples of BPSK signal and carrier signal samples using DDFS.

$$V_{BPSK}(T_{sam}.n).V_{car}(T_{sam}.n) =$$

$$= A\ .D(t).cos\left(\frac{2\pi.n.f_{car}}{f_{sam}} + \varphi_0\right)\ .cos\left(\frac{2\pi\ .n\ .f_{car}}{f_{sam}}\right) \qquad (10)$$

$$V_{BPSK}(T_{sam}.n).V_{car}(T_{sam}.n) =$$

$$= \frac{A\ .D(t)}{2} cos\left(\frac{4\pi.n.f_{car}}{f_{sam}} + \varphi_0\right) + \frac{A\ .D(t)}{2}\cos(\varphi_0)$$

4-The following component are removed using a digital low pass filter (LPF):

$$\frac{A\ .D(t)}{2} cos\left(\frac{4\pi.n.f_{car}}{f_{sam}} + \varphi_0\right) \qquad (11)$$

5- The output signal of the low pass filter (LPF):

$$V(n)_{dem} = \frac{A\ .D(t)}{2}\cos(\varphi_0) \qquad (12)$$

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6- Design the digital low pass filter (LPF) using MATLB and VHDL with the following parameters [7] :

-Type of filter : LPF .

- Filter structure : Direct form - FIR

-Filter order : 199.

-Filter length : 200.

-Sampling frequency : 40 KHz.

-Frequency of modulating signal : 0.25 KHz , 0.125 KHz.

-Cut-off frequency of LPF: 2 KHz.

-Window type : Hamming.

-Word length : 8 bits.

The specifications and the magnitude response of a digital filter designed in MATLAB [8] are shown in figure (3).

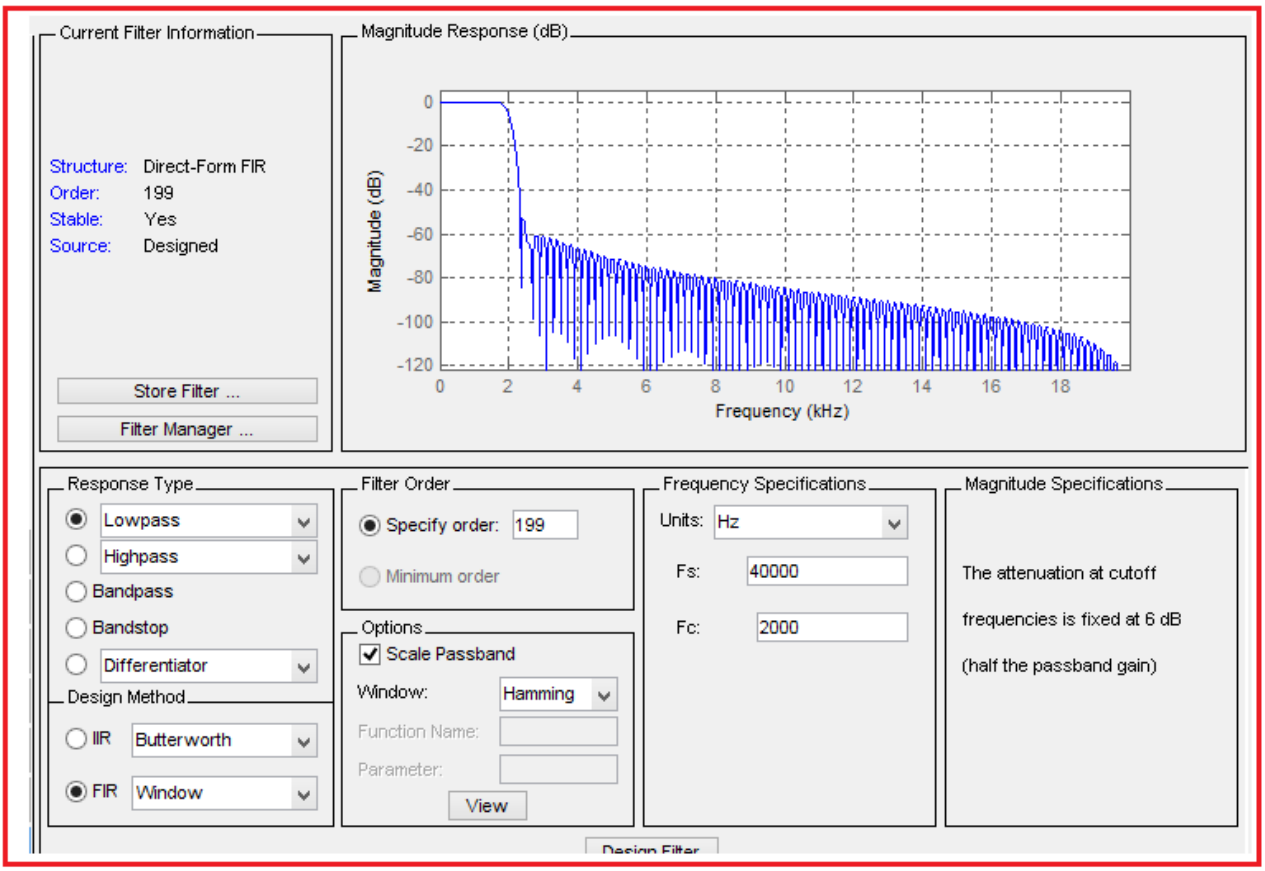

Fig (3) : The specifications and the magnitude response of a digital filter designed in MATLAB.

V. DESIGN OF THE DIGITAL BPSK DEMODULATOR USIGN DDFS IN QUARTUS II 9.1

We have a DDFS which has the following parameters:

-The frequency step is : $\delta f = 3\ Hz$, $F_{CLK} = 50\ MHz$.

-The modulating signal (MOD) is square pulse of frequency f_{mod1}=0.25 KHz ,f_{mod2}=0.125 KHz and frequency of carrier signal f_{car}=2 KHz.

-Modulation type: BPSK.

-The ROM capacity for the stored signal samples 8192X8 bits and their values are positive within the range from 0 to 255.

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-The number of the accumulator bits is computed from the following mathematical relation [9]:

$$\delta f = \frac{F_{CLK}}{2^n} \qquad (13)$$

$$\delta f = \frac{F_{CLK}}{2^n} \Longrightarrow 2^n = \frac{F_{CLK}}{\delta f} = \frac{50\ X\ 10^6}{3} = 24 \text{ bits}$$

-The frequency range for the carrier and modulating signals synthesizer is computed from the following mathematical relation [9]:

$$\Delta f = 0 \ldots\ldots \frac{F_{CLK}}{2} = 0 \ldots .25\ MHz$$

-To synthesize four signals of frequencies $f_{sam} = 40\ KHZ$, $f_{car} = 10$ KHz , $f_{mod1} = 0.25$KHz , $f_{mod2} = 0.125$KHz , the frequency code must be [9]:

$$Code\ F = L = \frac{f.2^n}{F_{CLK}} \qquad (14)$$

$$Code\ f_{sam} = L_{sam} = \frac{f_{sam}.2^n}{F_{CLK}} = \frac{40 \text{ x } 2^{24}}{50000} = 13422$$

$$Code\ f_{car} = L_{car} = \frac{f_{car}.2^n}{f_{sam}} = \frac{2 \text{ x } 2^{24}}{40} = 4194304$$

$$Code\ f_{mod1} = L_{mod} = \frac{f_{mod1}.2^n}{f_{sam}} = \frac{0.25\text{x } 2^{24}}{40} = 104858$$

$$Code\ f_{mod2} = L_{mod} = \frac{f_{mod2}.2^n}{f_{sam}} = \frac{0.125 \text{ x } 2^{24}}{40} = 52429$$

The functional diagram of a digital amplitude BPSK modulator and coherence digital BPSK demodulator in Quartus II 9.I design environment is shown in figure (4), it consists of :

-BPSK-DDFS is allocated for shaping a digital coherence BPSK signal.

-CAR-DDFS is allocated for shaping a digital carrier signal with frequency 2KHz.

-DATA-GEN is allocated for shaping a square pulse signal with frequency 0.25KHz and 0.125KHz.

-DEMODULATOR (digital coherence BPSK demodulator) is allocated for multiplying the BPSK signal and the carrier signal.

-LPF (digital low pass filter) is allocated for a selection modulating signal.

-Sampling signal generator is allocated for shaping a square pulse with frequency 40KHz.

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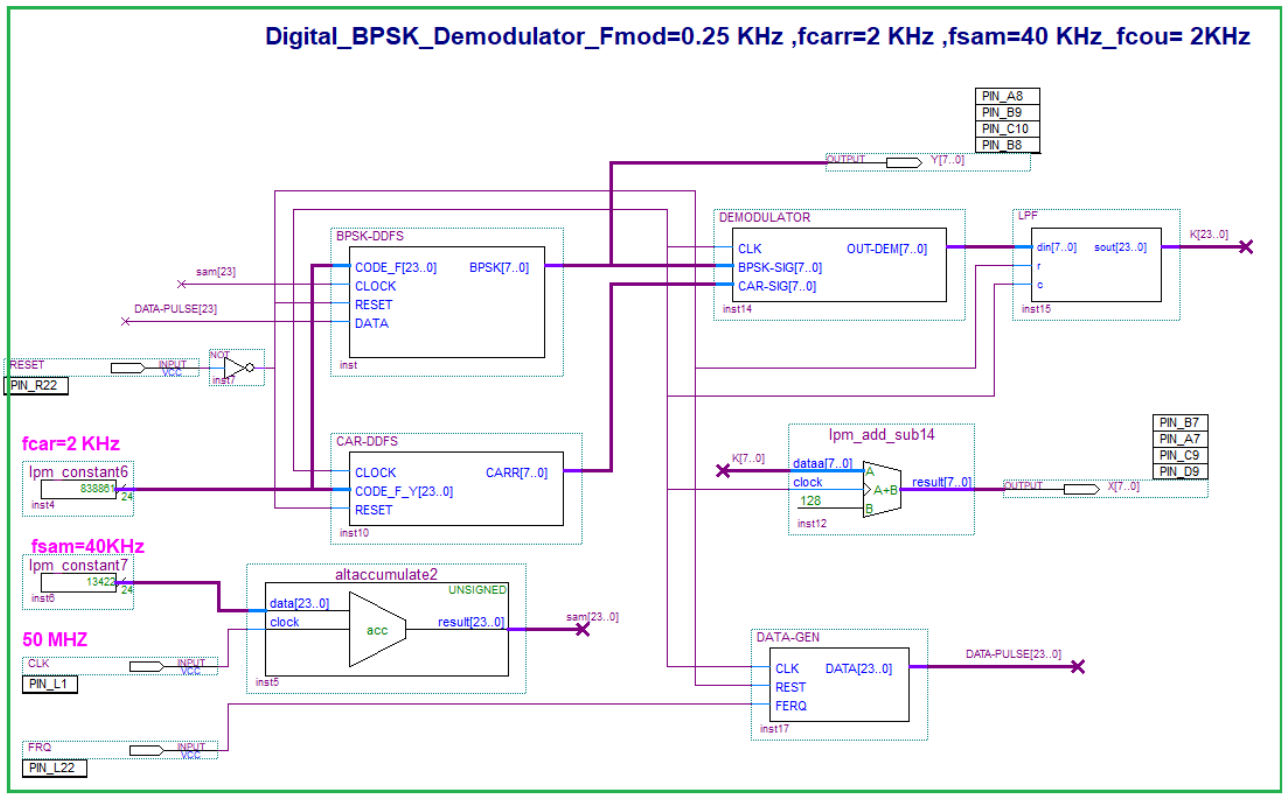

Fig (4) : The functional diagram of a digital BPSK modulator and coherence BPSK demodulator in Quartus II 9.I design environment

The block diagram of a digital BPSK- DDFS in Quartus II 9.I design environment is shown in figure (5).

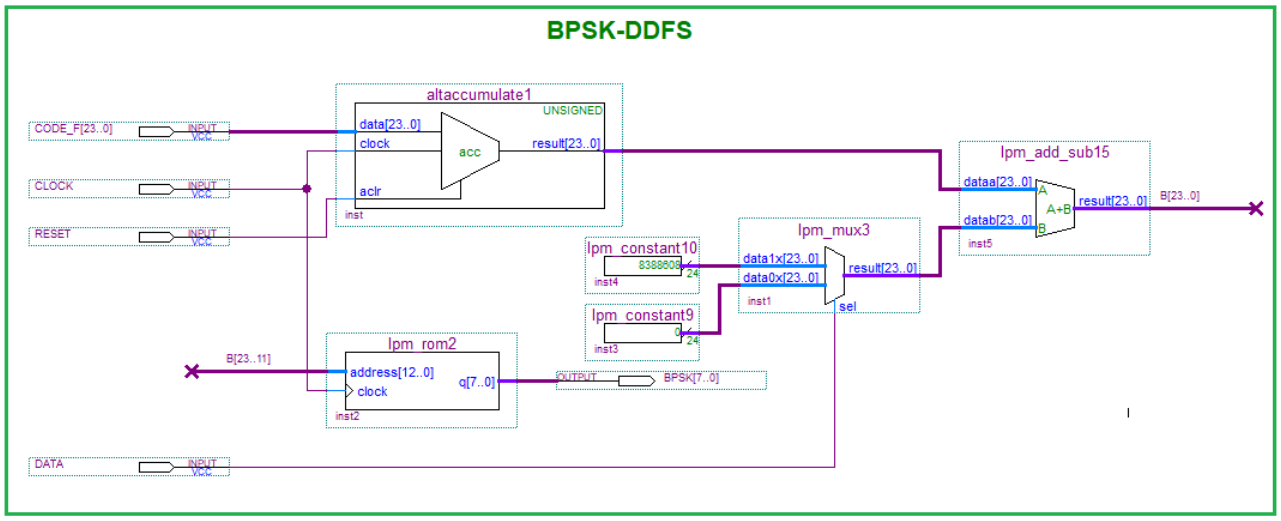

Fig (5) : The block diagram of a BPSK-DDFS in Quartus II 9.I design environment

The block diagram of a digital carrier DDFS in Quartus II 9.I design environment is shown in figure (6).

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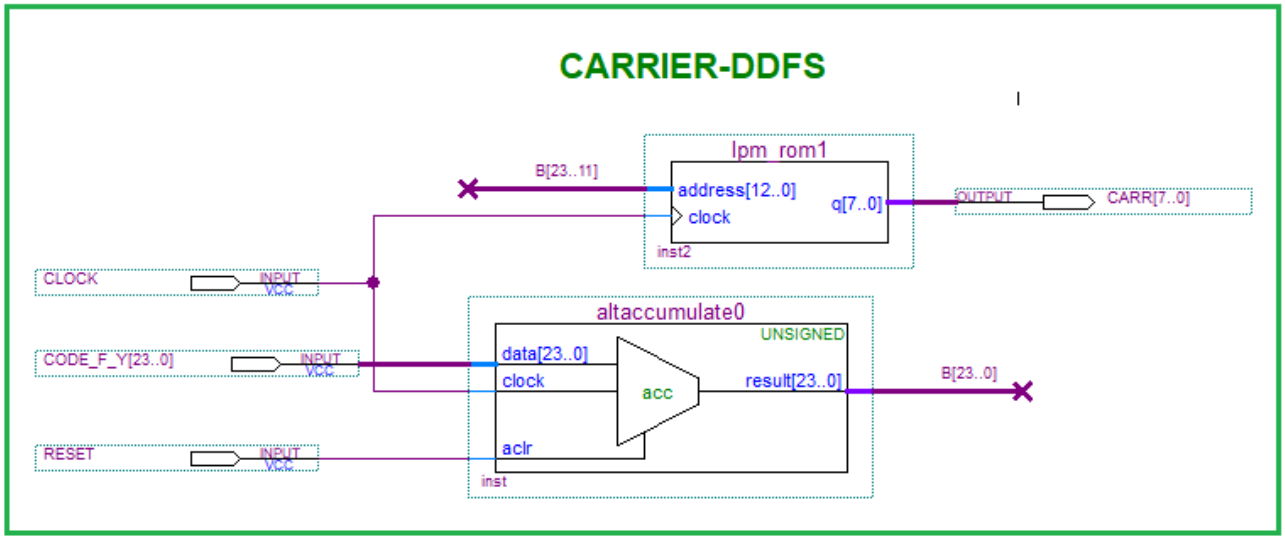

Fig (6) : The block diagram of a CARRIER-DDFS in Quartus II 9.I design environment

The results of the practical design of a digital sampling generator for f_{sam}=40 KHz and carrier DDS for f_{car}=2 KHz in time domain are shown in figure. (7).

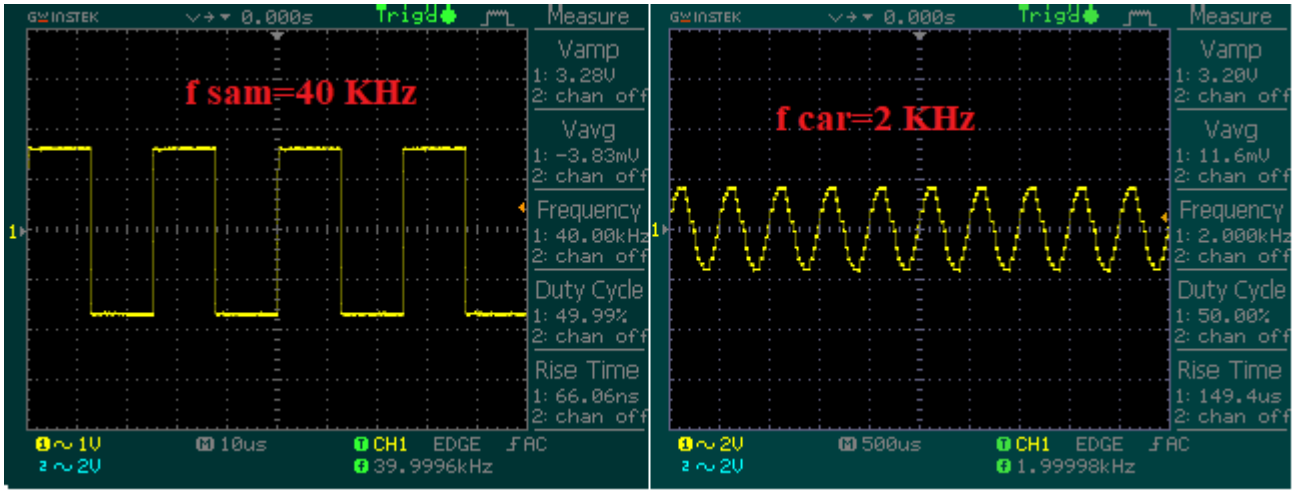

Fig. 7: The sampling signal for f_{sam}=40 KHz and carrier signal for f_{car} =2 KHz in time domain.

The results of the practical design of a digital sampling generator for f_{sam}=40 KHz and carrier DDS for f_{car}=2 KHz in frequency domain are shown in figure. (8).

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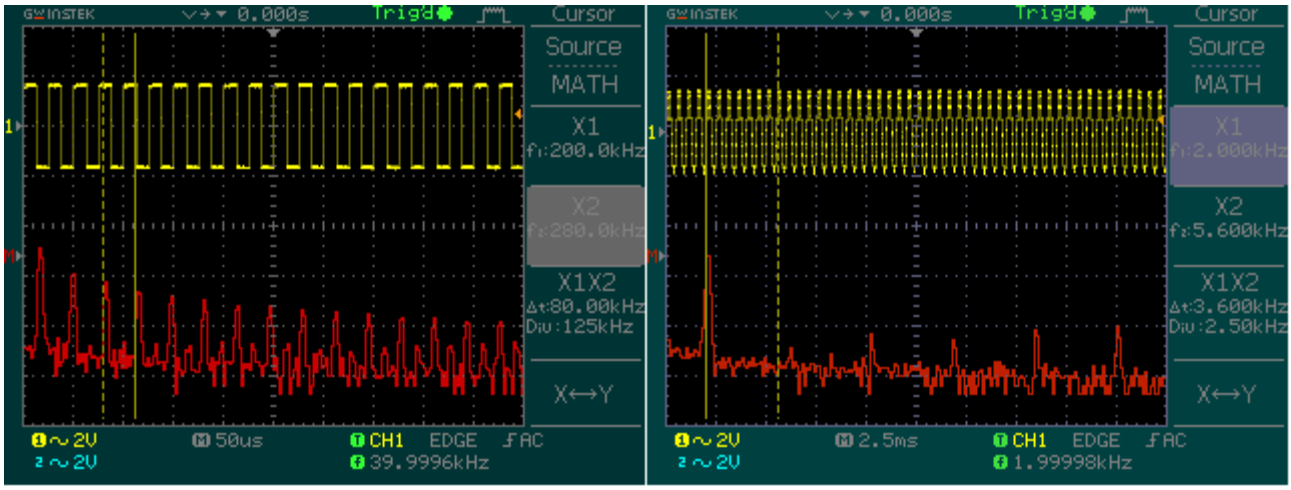

Fig. 8: The sampling for f_{sam}=40 KHz and carrier signal for f_{car} =2 KHz in frequency domain.

The block diagram of a digital BPSK demodulator in Quartus II 9.I design environment is shown in figure (9).

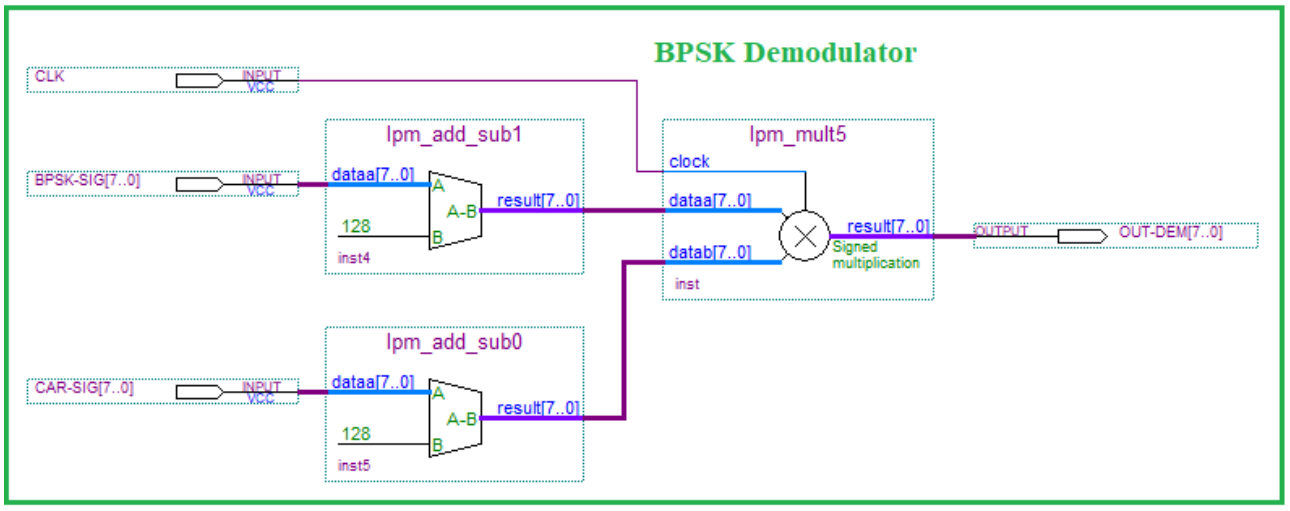

Fig (9) : The block diagram of a digital coherence BPSK demodulator in Quartus II 9.I design environment

The block diagram of a digital data generator for f_{mod1}=0.25 KHz and f_{mod2}=0.125 KHz in time domain according to the previous application using the FPGA chip placed on education and development board DE1 is shown in figure. (10).

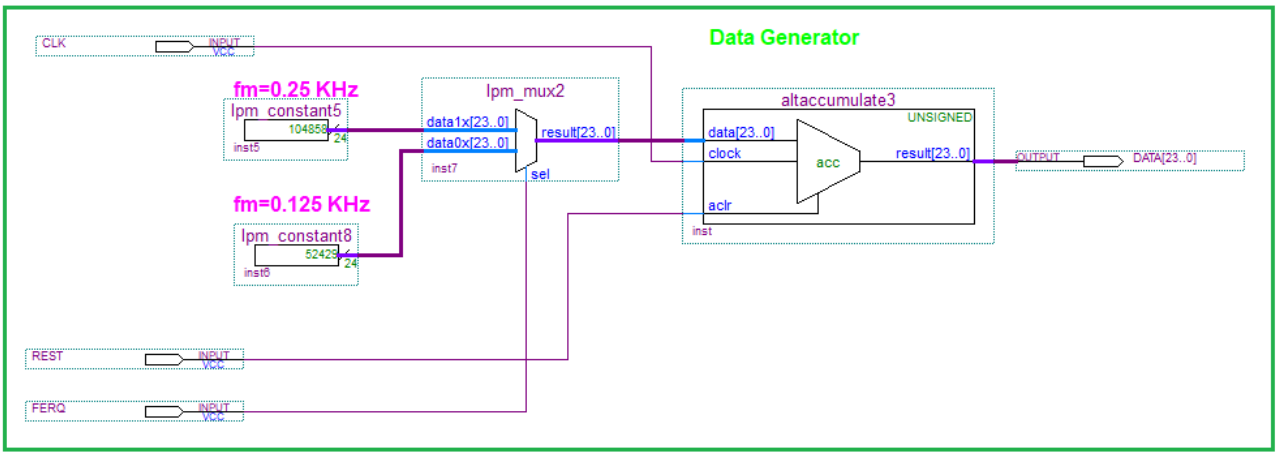

Fig (10) : The block diagram of a digital data generator in Quartus II 9.I design environment

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The results of the practical design of a digital data generator for f_{mod1}=0.25 KHz and f_{mod2}=0.125 KHz in time domain are shown in figure. (11).

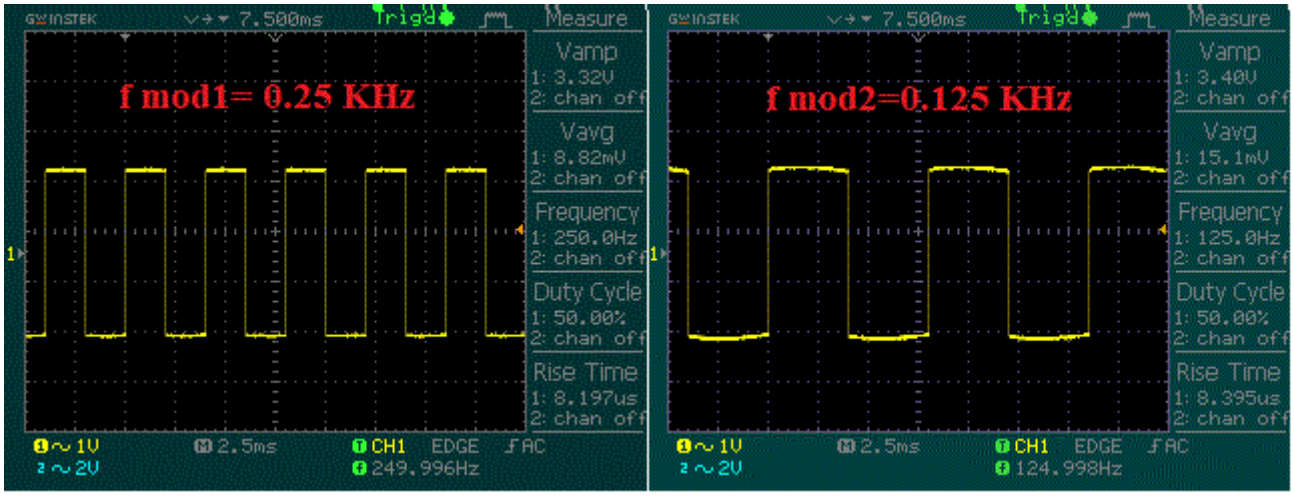

Fig. 11: The signals of digital data generator for f_{mod1}=0.25 KHz and f_{mod2} =0.125 KHz in time domain.

The results of the practical design of a digital data generator for f_{mod1}=0.25 KHz and f_{mod2}=0.125 KHz in frequency domain are shown in figure. (12).

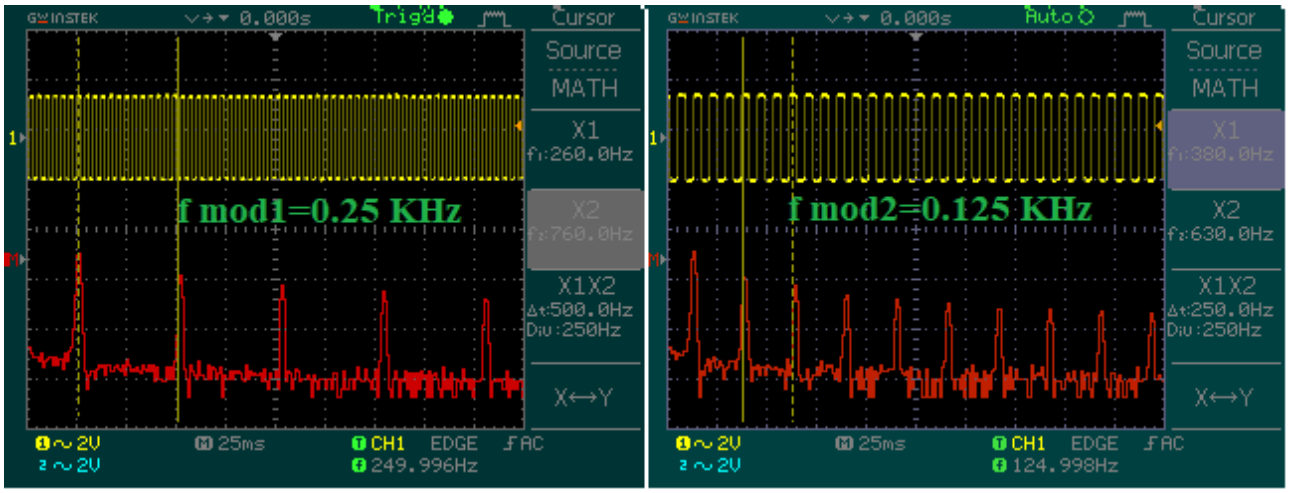

Fig. 12: The signals of digital data generator for f_{mod1}=0.25 KHz and f_{mod2} =0.125 KHz in frequency domain.

VI. RESULTS OF DESIGN

The results of the practical design for the digital BPSK demodulator for f_{mod1}=0.25 KHz , f_{mod2}=0.125 KHz and f_{car} =2 KHz in time domain according to the previous application using the FPGA chip placed on education and development board DE1 are shown in figure (13) and in figure (14) in frequency domain .

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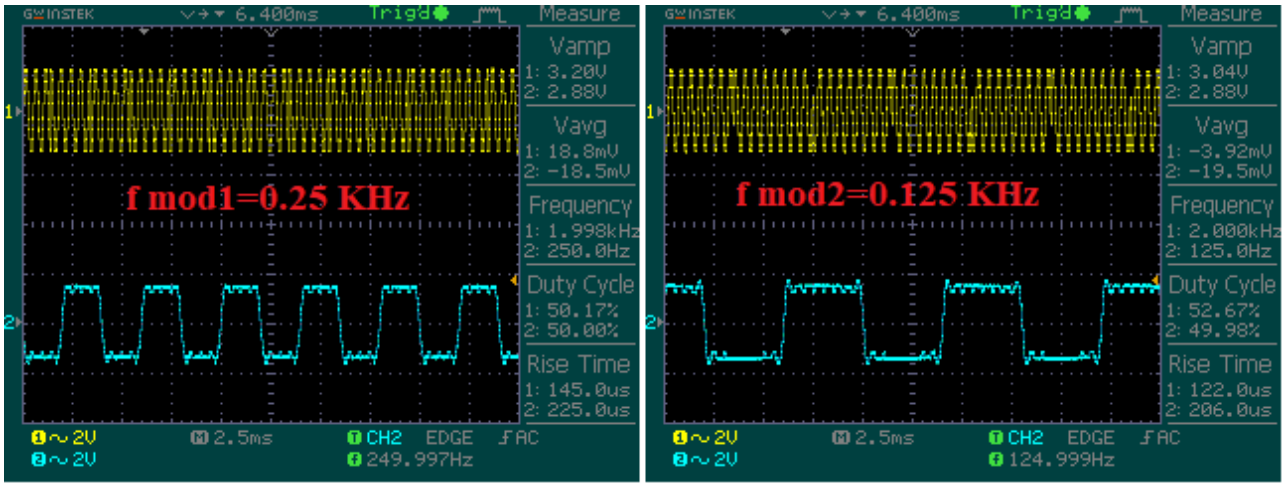

Fig. 13: The input and output BPSK demodulator signals for f_{mod1}=0.25 KHz and f_{mod2} =0.125 KHz in time domain.

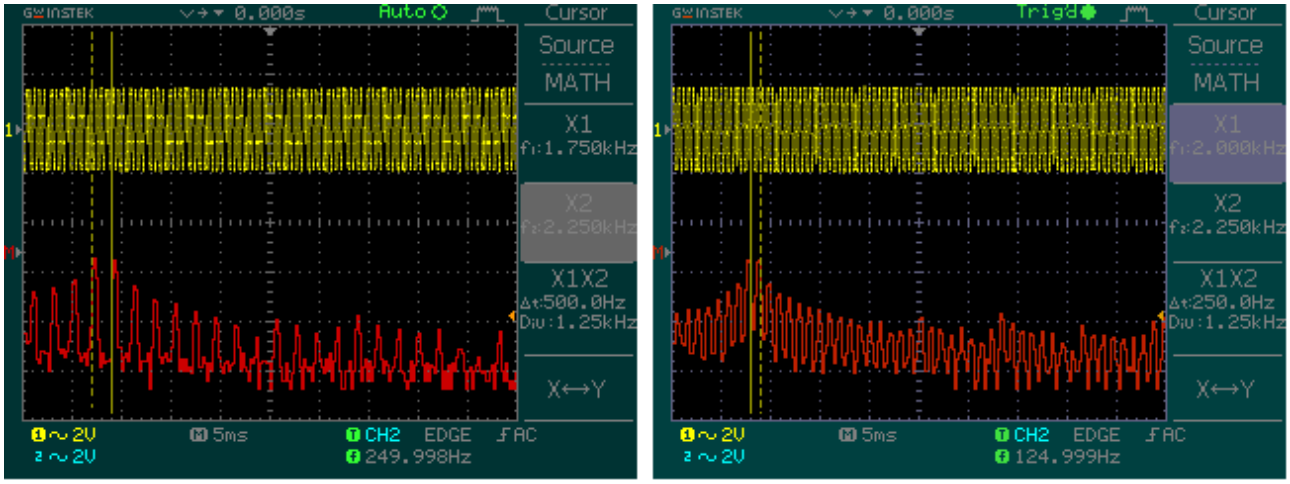

Fig. 14: The output BPSK demodulator signals for f_{mod1}=0.25 KHz and f_{mod2} =0.125 KHz in frequency domain.

These figures are taken from the screen of digital oscilloscope and digital spectrum analyzer , we can notice the identification between the theoretical results and the practical results, which indicate the high accuracy of digital synthesizing and demodulation operations for these signals.

VII. DISCUSSION AND CONCLUSIONS

-The use of high-order of FIR filters makes the digital filtering process of the demodulator accurate and efficient.
-The higher order of FIR , the more unwanted frequency components are removed, thus improving the demodulation process.
-Using DDFS techniques in communication domain allows implementing different digital modulation and demodulation operations with high accuracy and speed in digital signal synthesizing, and with the ability of changing parameters in wide range.
-Using DDFS techniques in communication domain allows implementing the digital processing in the communication receiver on high intermediate frequency.
-We notice from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital synthesizing and modulation operations for signals.
-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).
-The most important thing in this paper is the possibility of changing the frequency of the modulating signal ,frequency of data generator and the frequency of the carrier signals.

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BIOGRAPHY

Dr. Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR , university of communication in Leningrad , holds a degree assistant professor in 2009 from Aleppo university. Lecturer at Department of Biomedical Engineering , Al Andalus University For Medical Sciences-Syria ,Tishreen University-Syria ,Corduba Private University- Syria , Kassala University-Sudan and Ittihad Private University- Syria.

Published a lot of researches in the field of digital communication and digital signal processing in the universities journals of Syria and in the European and Indian journals.

Working in the field of programming FPGA by using VHDL, and design of Digital Filters.