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Design and Implementation of a Digital Binary Phase Shift keying (BPSK) Synthesizer For Radar Signal With Barker Codes Using FPGA

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Abstract

This paper proposes the design and implementation of the mechanism of digital synthesizing for BPSK pulses according to Barker codes of 5, 7, 11, and 13 chips practically using a digital programmable device Cyclone II EP2C20F484C7 FPGA from ALTERA, placed on education and development board DE-1 according to the following parameters:

- The carrier frequency: $F_c = 1\ MHz$.
- Modulation type: BPSK according to Barker code.
- Sampling frequency :$\left(F_{samp} = 50\ MHz\ , T_{samp} = 0.02\ \mu sec\right)$.
- Pulse repetition period is : $(T = 200\ \mu sec)$.
- Pulse width is : $(\tau = 5\ ,7\ ,11\ ,13\ \mu sec)$.
- The single chip width is : $(\tau_{CH} = 1\mu\,\text{sec}\ \ , F_{CH} = 1\ MHz)$.
- Chips number is : 5, 7, 11, and 13.
- Frequency resolution is : $\delta f = 762Hz$.
- The results of the filter operation are studied using a digital oscilloscope GDS-1052U for the radar signal of the shown specifications.

-All variable parameters are computer – controlled, with BPSK or without BPSK, $(f_0, N\ , \tau\ , \tau_{CH}\ , T)$

Keywords: BPSK , Barker Code , DDFS, FPGA.

I. INTRODUCTION

BPSK signals are widely used in radar technology because they have the feature of increasing the pulse width in the transmitter to increase the radar range, and compressing the pulse in the receiver to achieve high range-resolution In this paper we designed and implemented the mechanism of digital synthesizing for BPSK pulses with 5,7,11 and 13 chips of Barker Code, using a digital programmable device The parameters of the BPSK generated signal are analyzed using a digital oscilloscope and spectrum analyzer GDS-1052U.

The BPSK signal according to Barker codes is given by the following mathematical relation [1]:

$$S_{BPSK}(t) = A(t)\sum_{i=1}^{N} g_i \cos[w_0 t] \qquad (1)$$

Where:

$$(g_i) = \pm 1$$

$$A(t) = \begin{cases} 1 \ \ for\ 0 \le t \le \ \tau \\ 0\ for\ another\ t \end{cases} \qquad (2)$$

For g(n)= +1, the initial phase for $S_{BPSK}(t)$signal equals (0) and for g(n)= -1, the initial phase for $S_{BPSK}(t)$ signal equals (π) .

N: The chips number of the code (5, 7, 11, 13).

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The Barker codes are given according the table (1) and the time diagram of the BPSK signal according to Barker code is shown in the figure. 1 for two cases (N=5, N=7).

The BPSK is implemented according to Barker codes using DDFS as shown in the figure. 2 which consists of DDFS, radar pulses synthesizer to synthesizing the pulse modulating signal of repetition period (T) and width(τ), Barker code chips synthesizer of the required chips number (N) to synthesizing BPSK, the functional diagram of the BPSK modulator according to Barker codes is shown in the figure. 3.

-The number of the accumulator bits is computed from the following mathematical relation [2]:

$$\delta f = \frac{F_{CLK}}{2^n} \Rightarrow 2^n = \frac{F_{CLK}}{\delta f} = \frac{50 \text{ x } 10^6}{762} \Longrightarrow n = 16 \ \ bits$$

-The frequency range for the synthesizer is computed from the following mathematical relation:

$$\Delta f = 0 \ldots \frac{F_{CLK}}{2} = 0 \ldots .25 \ MHz$$

The frequency code of the synthesizer due to pulse modulation is computed according the following mathematical relation

$$Code \ F_c = L_1 = \frac{2^n \ F_c}{F_{CLK}} \qquad (3)$$

$$Code \ 0 = L_2 = \frac{2^n \text{ x } 0}{F_{CLK}} = 0$$

-To synthesize a signal of F_c=1 MHZ, the corresponding frequency code must be equal to:

$$Code \ F_c = L_1 = \frac{2^n \ F_c}{F_{CLK}} = \frac{2^{16} \text{ x } 1}{50} = \frac{65536}{50} = 1311$$

-To synthesize the signal of initial phase 0 or 180 degree, the corresponding phase codes must be equal to [3]:

$$Code \ Phase = X_\varphi = \frac{2^n \ \varphi}{2\pi} \qquad (4)$$

$$Code \ Phase \ \ 0 = X_0 = 0$$

$$Code \ Phase \ \ 180 = X_{180} = \frac{2^n \ \pi}{2\pi} = \frac{2^n}{2} = \frac{2^{16}}{2} = 32768$$

Table (1) Barker codes structure according to chips number

N	Chips												
	1	2	3	4	5	6	7	8	9	10	11	12	13
5	+1	+1	+1	-1	+1								
7	+1	+1	+1	-1	-1	+1	-1						
11	+1	+1	+1	-1	-1	-1	+1	-1	-1	+1	-1		
13	+1	+1	+1	+1	+1	-1	-1	+1	+1	-1	+1	-1	+1

Where:

n: the synthesizer DDFS accumulator capacity which define the step of synthesizer tuning.

F_{CLK}: the clock pulses frequency of the DDFS.

F_c : the DDFS carrier frequency.

φ : phase of a BPSK signal.

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The pulse modulating signal (Pulse Mod) is considered as a pulses of repetition period T and width $(\tau = N.\tau_{CH})$, using digital pulse synthesizer DPS if the Pulse Mod signal equals "1" the (Code F_c) is passed through the multiplexer MUX-BUS to the synthesizer to synthesize the frequency (F_c) during the time of pulse width, and if Pulse Mod signal equals "0" the Code 0 is passed through the MUX-BUS to the synthesizer to synthesize the signal $(F_c = 0)$ during the time of no pulse (τ).

The phase modulating signal (Phase Mod) is considered as a pulses of repetition period T with the same pulses repetition period of the pulse modulation (Pulse Mod) and width (τ_{CH}) for the single chips, the chips number and their values are shown in the previous table. If the Phase Mod signal equals "1" the Code Phase 0 is passed through the multiplexer MUX-BUS to the synthesizer to synthesize the signal $[sin(2\pi t)]$ figure 3 with initial phase 0 during the time of "1" pulse, and if Phase Mod signal equals "0" the Code Phase (π) or (180^0) is passed through the MUX-BUS to the synthesizer to synthesize the signal $[sin(2\pi t + \pi)]$ with initial phase (π) during the time of "0" pulse as the situation in BPSK.

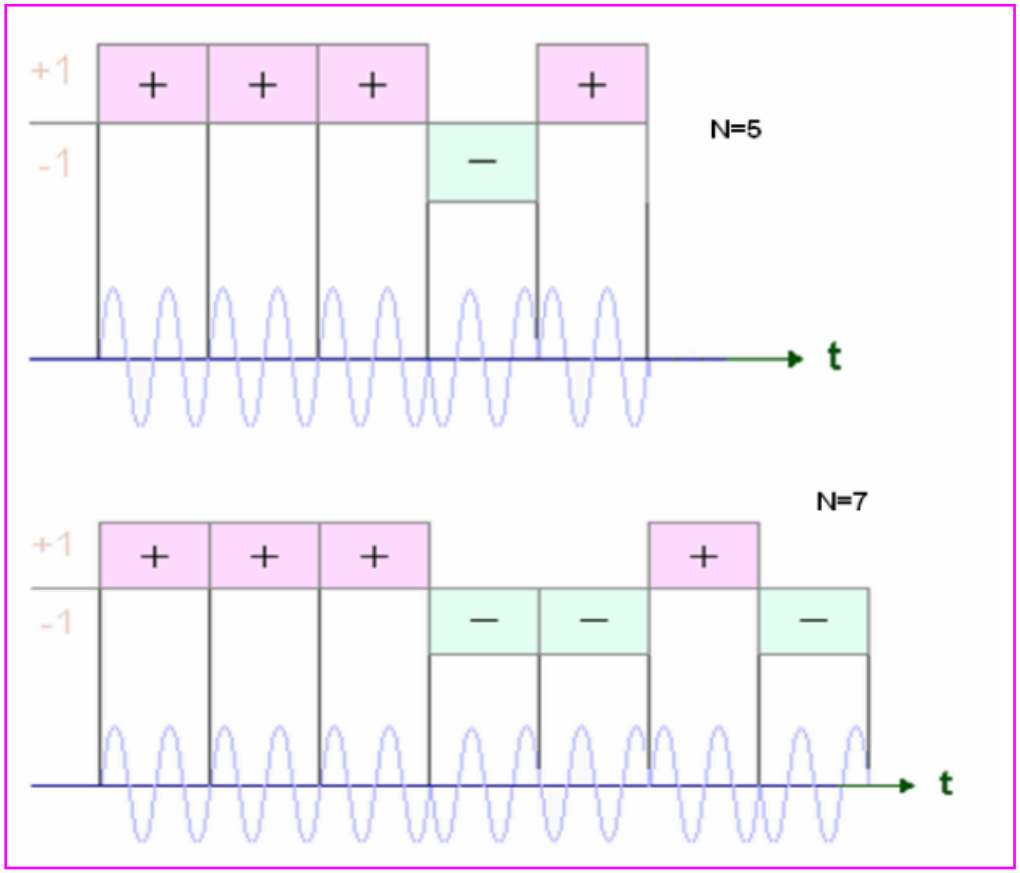

Fig. 1: The time diagram of the BPSK signal according to Barker code in case of N=5, and N=7

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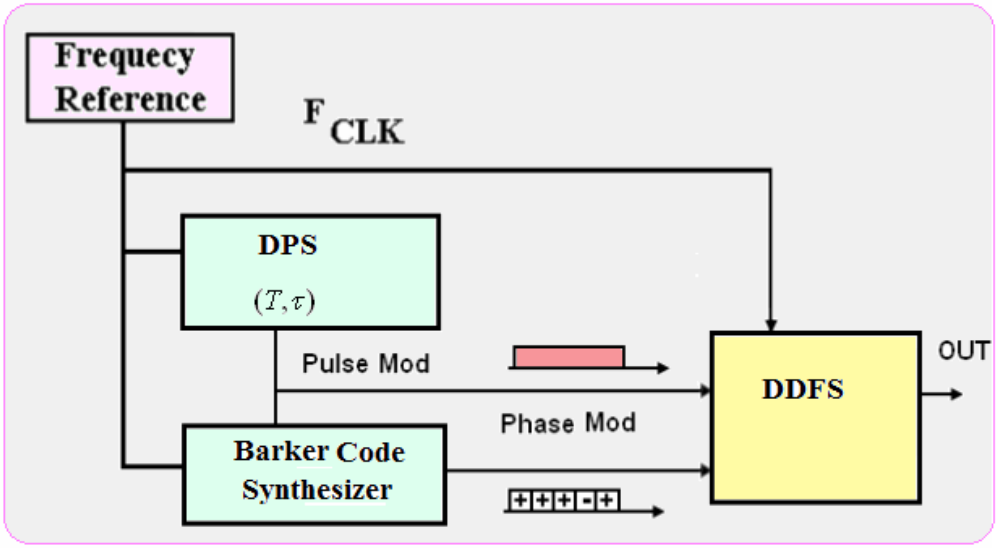

Fig. 2: The block diagram of the digital BPSK modulator according to Barker code using DDFS

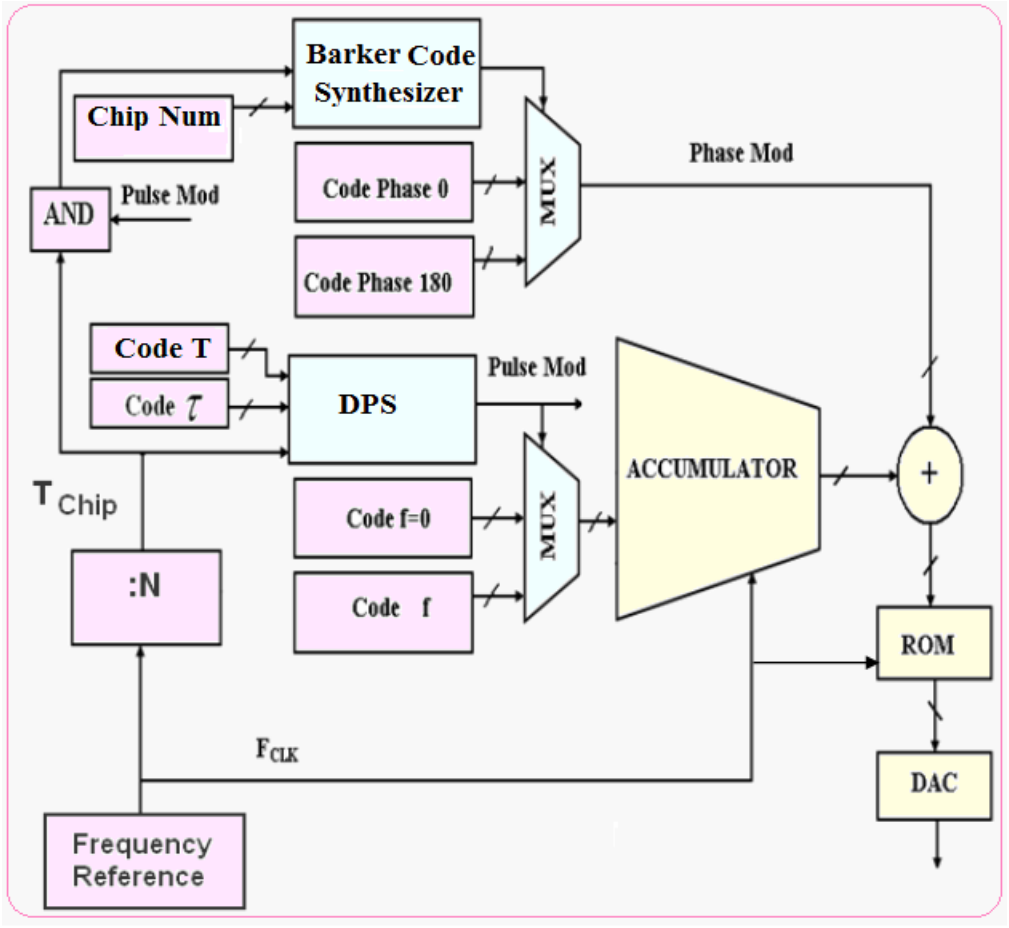

Fig. 3: The functional diagram of the BPSK modulator according to Barker code using DDFS

II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

Research Importance:

The importance of this research lies in advanced digital solution for radar systems , where the BPSK signal synthesizer using Barker codes length $(5,7,11,13)$ via DDFS and DPS on FPGA provides high-precision signals with excellent side lobe suppression .

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This enhances jamming resistance and energy efficiency in detection and surveillance applications , utilizing a $(1\ \mu sec)$ chip width , $(50\ MHZ)$ sampling rate , $(1\ MHZ)$carrier, and $(T = 200\ \mu sec)$pulse repetition period.
The FPGA implementation offers high flexibility and low cost , supporting application in resource –limited setting.

Research Objectives:

1-Design and implement a BPSK synthesizer using Barker codes of length $(5,7,11,13)$ via DDFS and DPS on FPGA.
2-Achive a $(1\ \mu sec)$, $(50\ MHZ)$ sampling rate , $(1\ MHZ)$carrier , and $(T = 200\ \mu sec)$pulse repetition period with high accuracy.
3-Evalute signal performance in side-lobe suppression and jamming resistance for radar application.
4-Compare efficiency with traditional methods and optimize the digital implementation.

III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the Digital Binary Phase Shift keying (BPSK) Synthesizer For Radar Signal with 5,7,11 13 chips of Barker code, the following tools and software are used:
- Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [4].
-DDFS for BPSK signal with Barker codes of 5,7,11,13 chips designed on FPGA chips.
-DPS for pulse signal with pulse repetition period is : $(T = 200\ \mu sec)$ and pulse width is : $(\tau = 5\ ,7\ ,11\ ,13\ \mu sec)$.
-VHDL programming language with Quartus II 9.I design environment [5].
- Design Environment MATLAB R2008a.
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.

IV. BLOCK DIAGRAM OF THE DIGITAL SYNTHESIZERS FOR THE BARKER CODES OF (5) CHIPS.

The general principle of synthesizing the Barker codes depends on using looping shift registers where the required sequence code is recorded and then rotates it within the shift register by clock pulses, which their period defines the single chip width (this repetition period always equals $1\mu sec$) , the recorded sequence code value expresses the synthesized Barker code (this easy and simple way to synthesizing Barker codes and not unique).
The functional diagram of the Barker code synthesizer due to N=5 is shown in the figure. 4 where the value of the stored code in the shift register (X=29) and the shift is to the left (Left Shift), figure. 5 shows the detailed diagram for this synthesizer using the programming environment Quartus II 9.1. figure. 6 shows the simulation results [6].

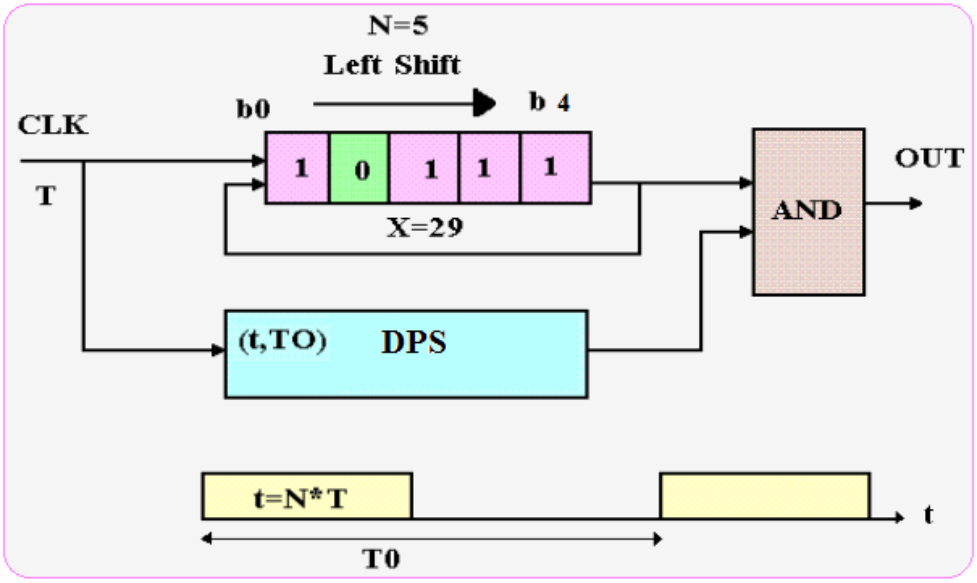

Fig. 4: The functional diagram of the Barker code synthesizer using shift register (case N=5)

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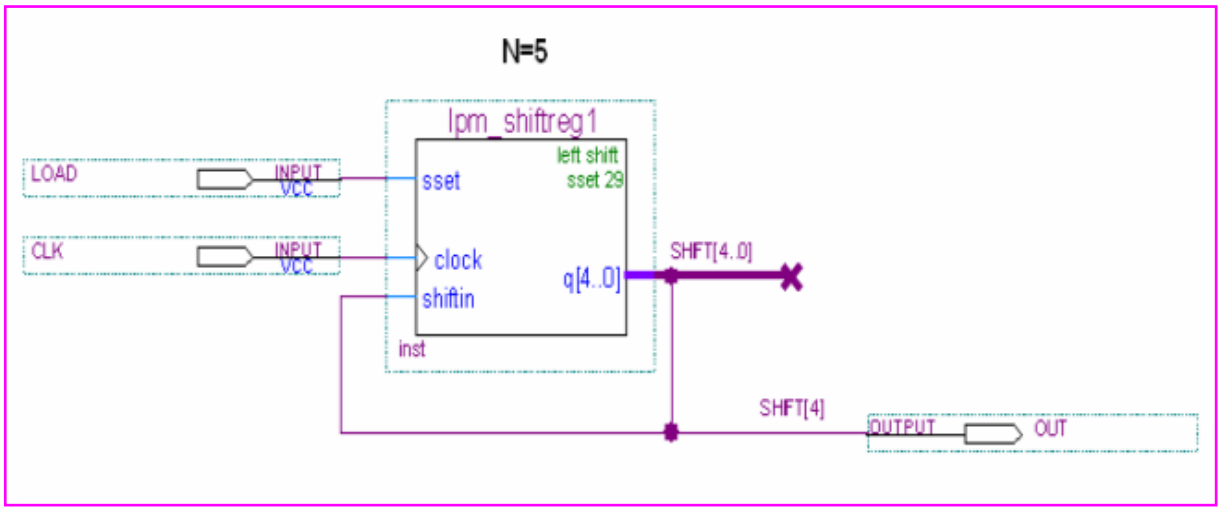

Fig. 5: The functional diagram of the Barker code synthesizer with five chips (N=5)

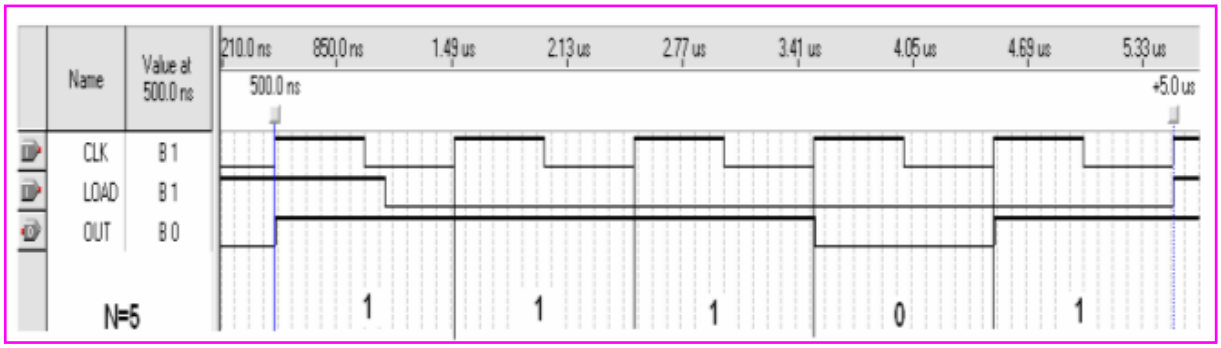

Fig. 6: The time diagram of the Barker code signal with five chips (N=5)

V. BLOCK DIAGRAM OF THE DIGITAL SYNTHESIZERS FOR THE BARKER CODES OF (7) CHIPS.

The functional diagram of the Barker code synthesizer due to N=7 is shown in the figure. 7 where the value of the stored code in the shift register (X=114) and the shift is to the left (Left Shift) [7] , figure. 8 shows the detailed diagram for this synthesizer using the programming environment Quartus II 9.1. figure. 9 shows the simulation results.

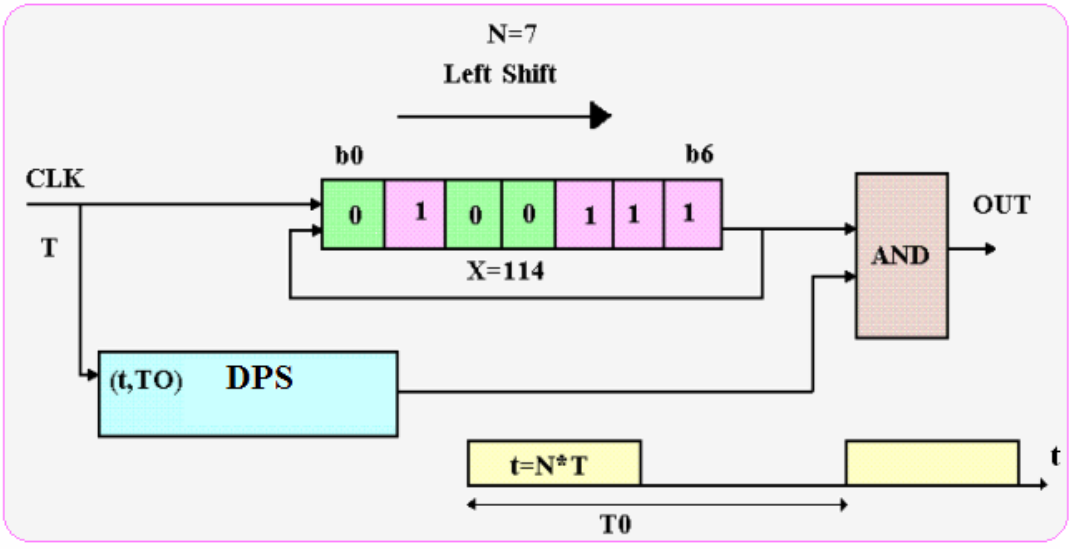

Fig. 7: The functional diagram of the Barker code synthesizer using shift register (case N=7)

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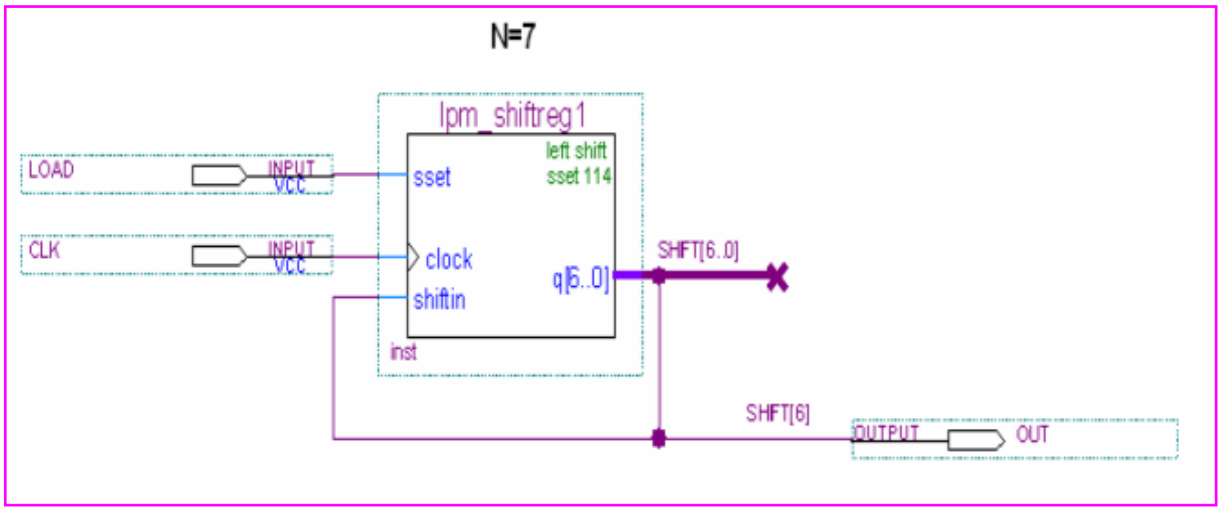

Fig. 8: The functional diagram of the Barker code synthesizer with seven chips (N=7)

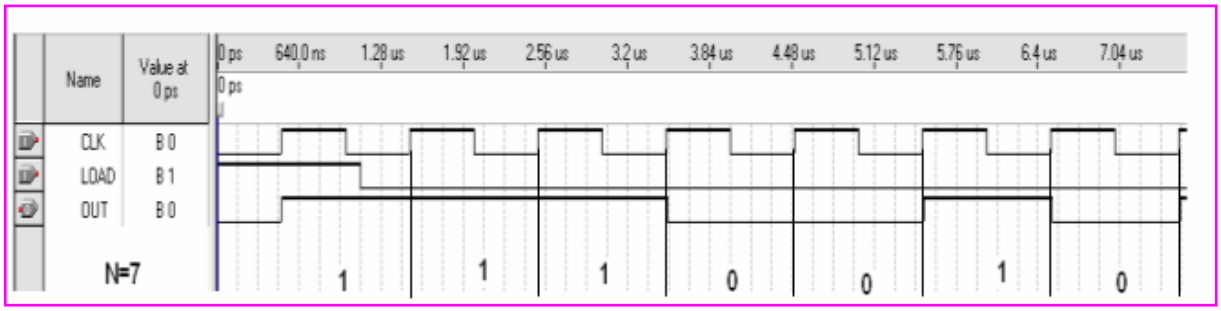

Fig. 9: The time diagram of the Barker code signal with seven chips (N=7)

V. BLOCK DIAGRAM OF THE DIGITAL SYNTHESIZERS FOR THE BARKER CODES OF (11) CHIPS.

The functional diagram of the Barker code synthesizer due to N=11 is shown in the figure. 10where the value of the stored code in the shift register (X=1810) and the shift is to the left (Left Shift), figure. 11 shows the detailed diagram for this synthesizer using the programming environment Quartus II 9.1. figure. 12 shows the simulation results.

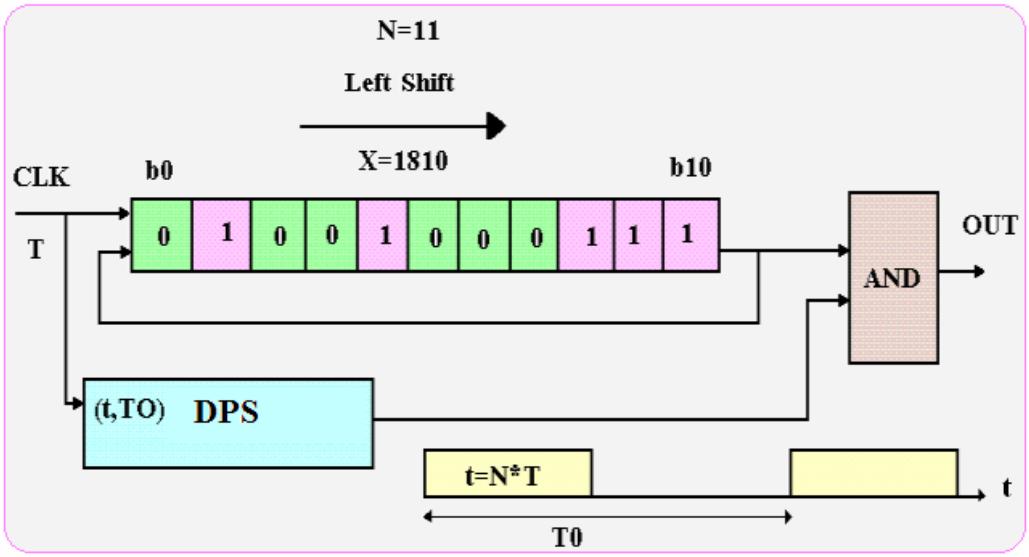

Fig. 10: The functional diagram of the Barker code synthesizer using shift register (case N=11)

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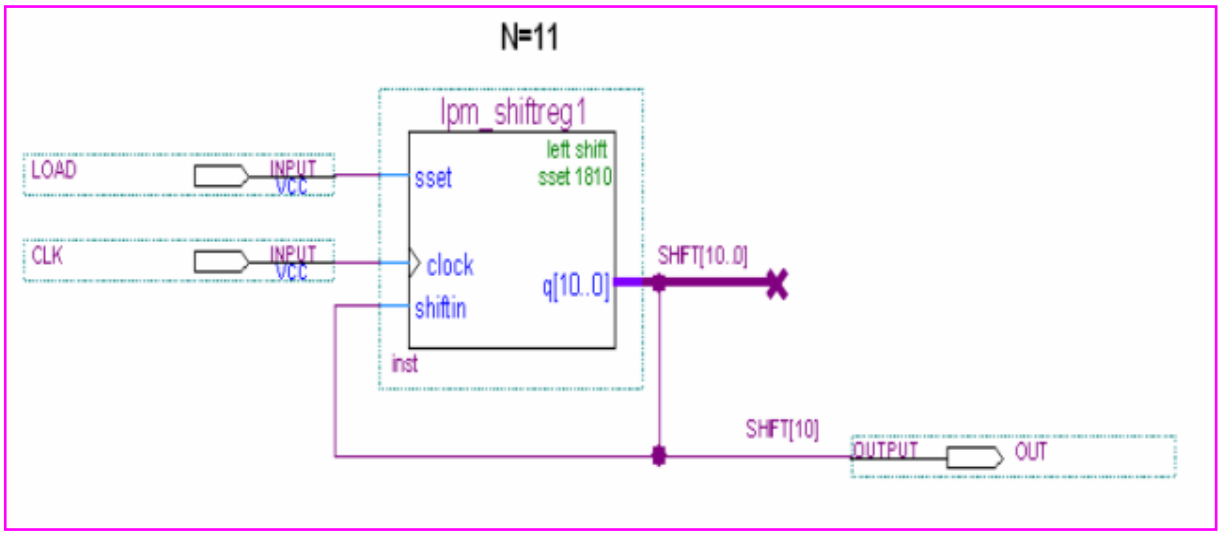

Fig. 11: The functional diagram of the Barker code synthesizer with eleven chips (N=11)

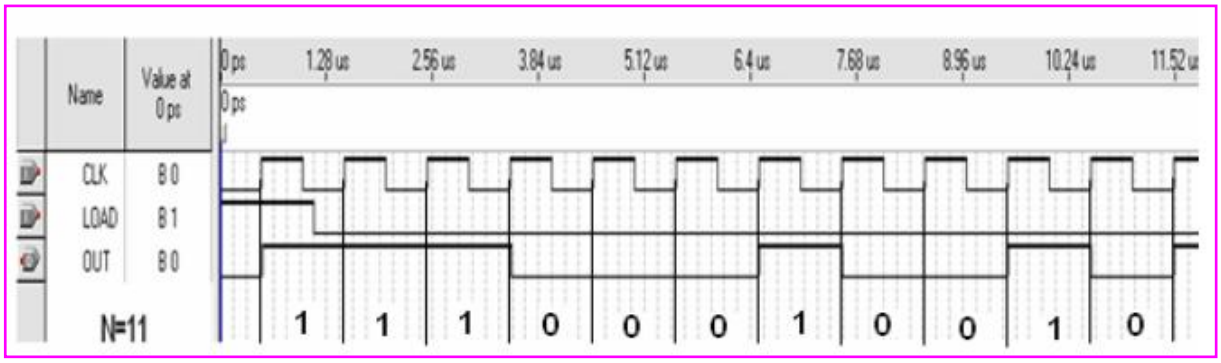

Fig. 12: The time diagram of the Barker code signal with eleven chips (N=11)

VI. BLOCK DIAGRAM OF THE DIGITAL SYNTHESIZERS FOR THE BARKER CODES OF (13) CHIPS.

The functional diagram of the Barker code synthesizer due to N=13 is shown in the figure.13 where the value of the stored code in the shift register (X=7989) and the shift is to the left (Left Shift), figure. 14 shows the detailed diagram for this synthesizer using the programming environment Quartus II 9.1. figure. 15 shows the simulation results.

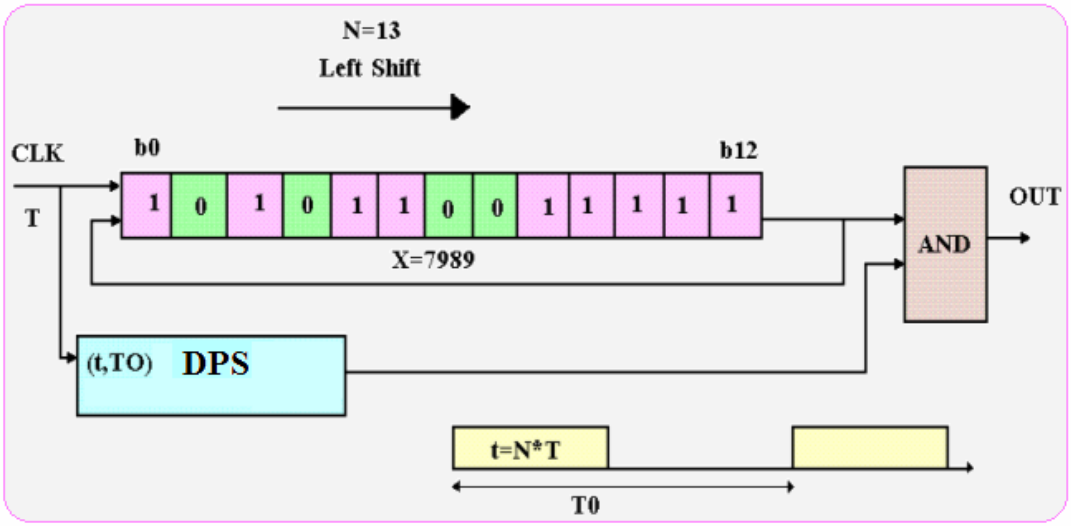

Fig. 13: The functional diagram of the Barker code synthesizer using shift register (case N=13)

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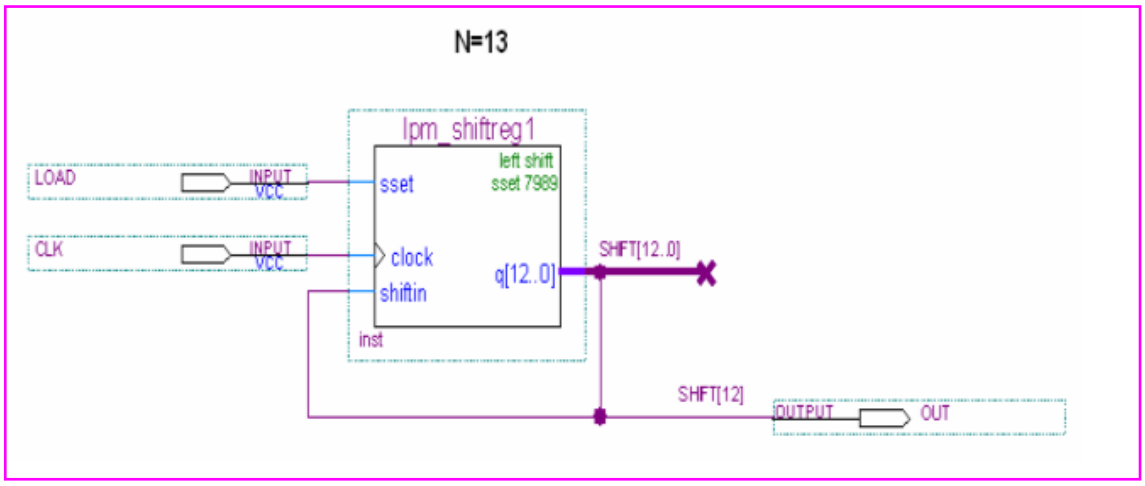

Fig. 14: The functional diagram of the Barker code synthesizer with thirteen chips (N=13)

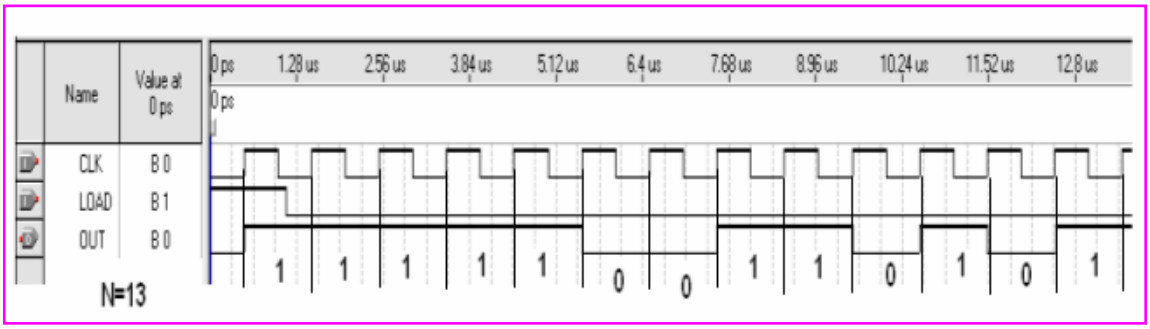

Fig. 15: The time diagram of the Barker code signal with thirteen chips (N=13)

VII. BLOCK DIAGRAM OF THE BPSK MODULATOR FOR THE BARKER USING THE PROGRAMMING ENVIROMENT QUARTUS II 9.1.

-The functional diagram of modulator BPSK according to Barker code using the programming environment Quartus II 9.1 is shown in figure. 16 for the frequency of ($F_c = 1MHz$) and this corresponds a frequency code of (L=1311), initial phase 0 degree which represents a phase code of 0, and initial phase 180 degree which represents a phase code of (32768) [8] .

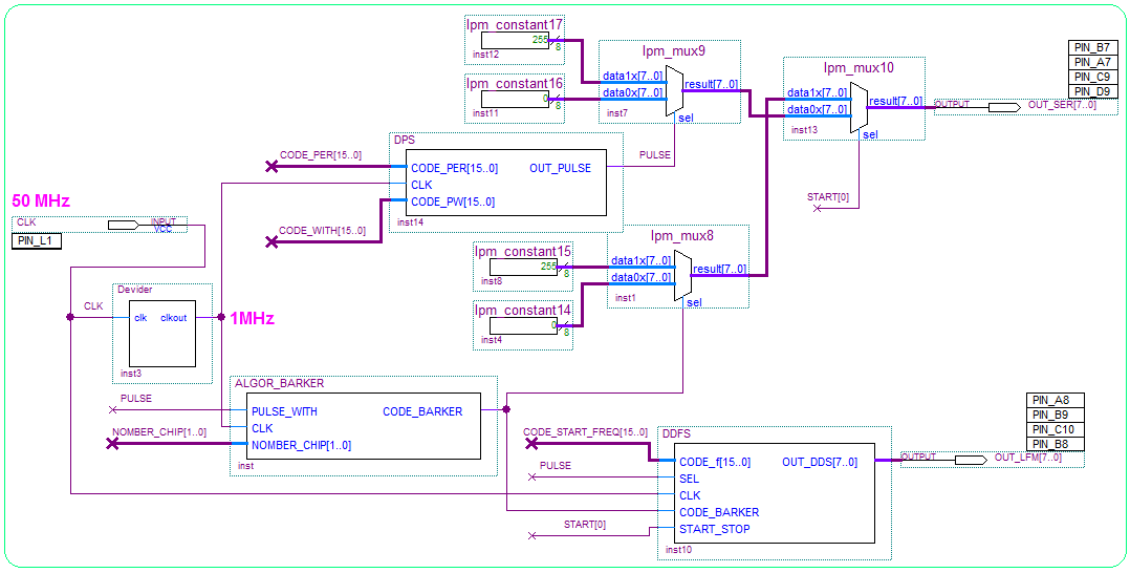

Fig. 16: The functional diagram of the BPSK modulator according to Barker code using DDFS

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-The functional diagram of the Barker codes synthesizer of chips (N=5, 7, 11, 13) to synthesizing the binary phase modulation pulses (Phase mod), using the programming environment Quartus II 9.1 is shown in the figure. 17.

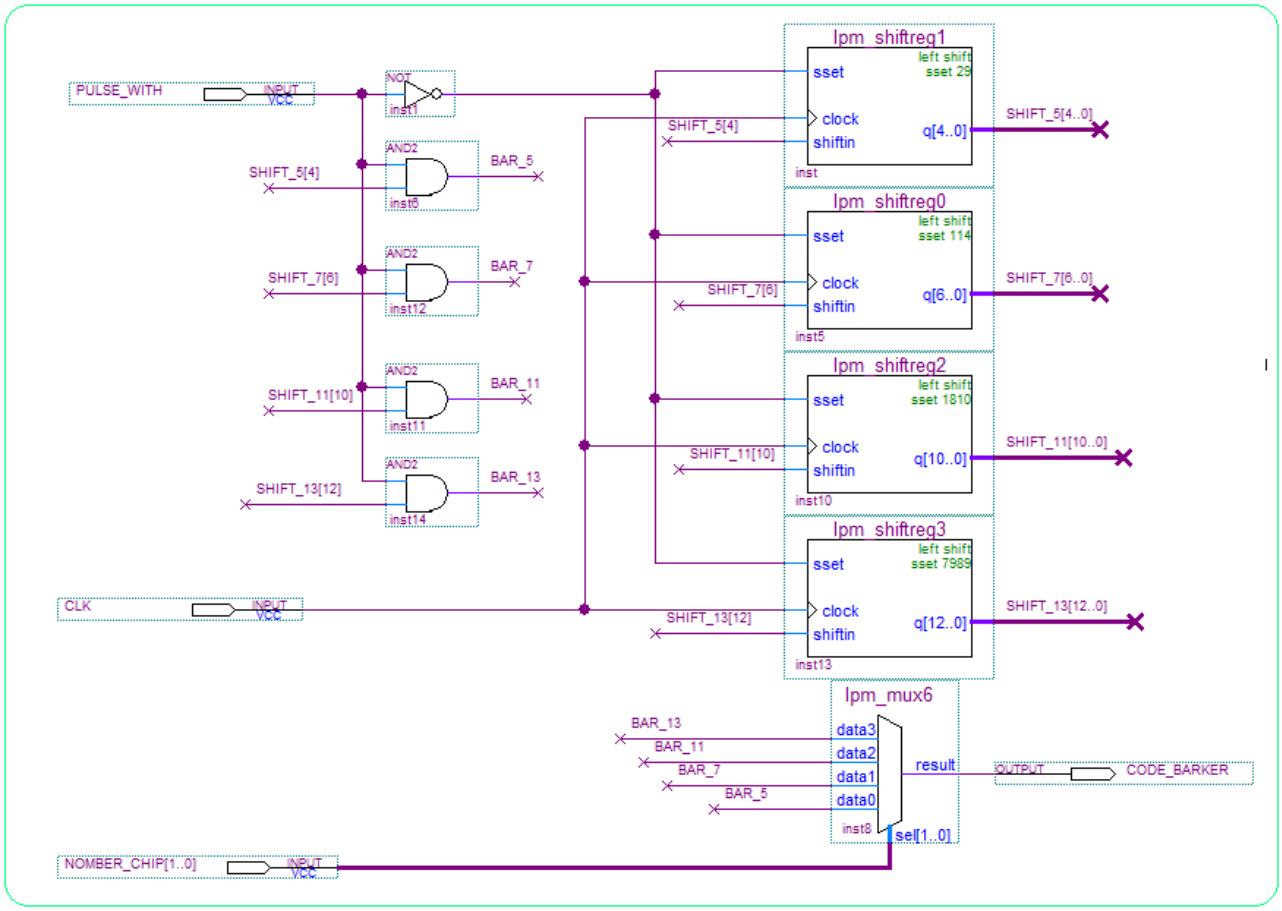

Fig. 17: The block diagram of the Barker codes synthesizer (N=5, 7, 11, 13)

-The functional diagram of the pulse and phase modulator using DDFS using the programming environment QUARTUS II 9.1 is shown in the figure.18.

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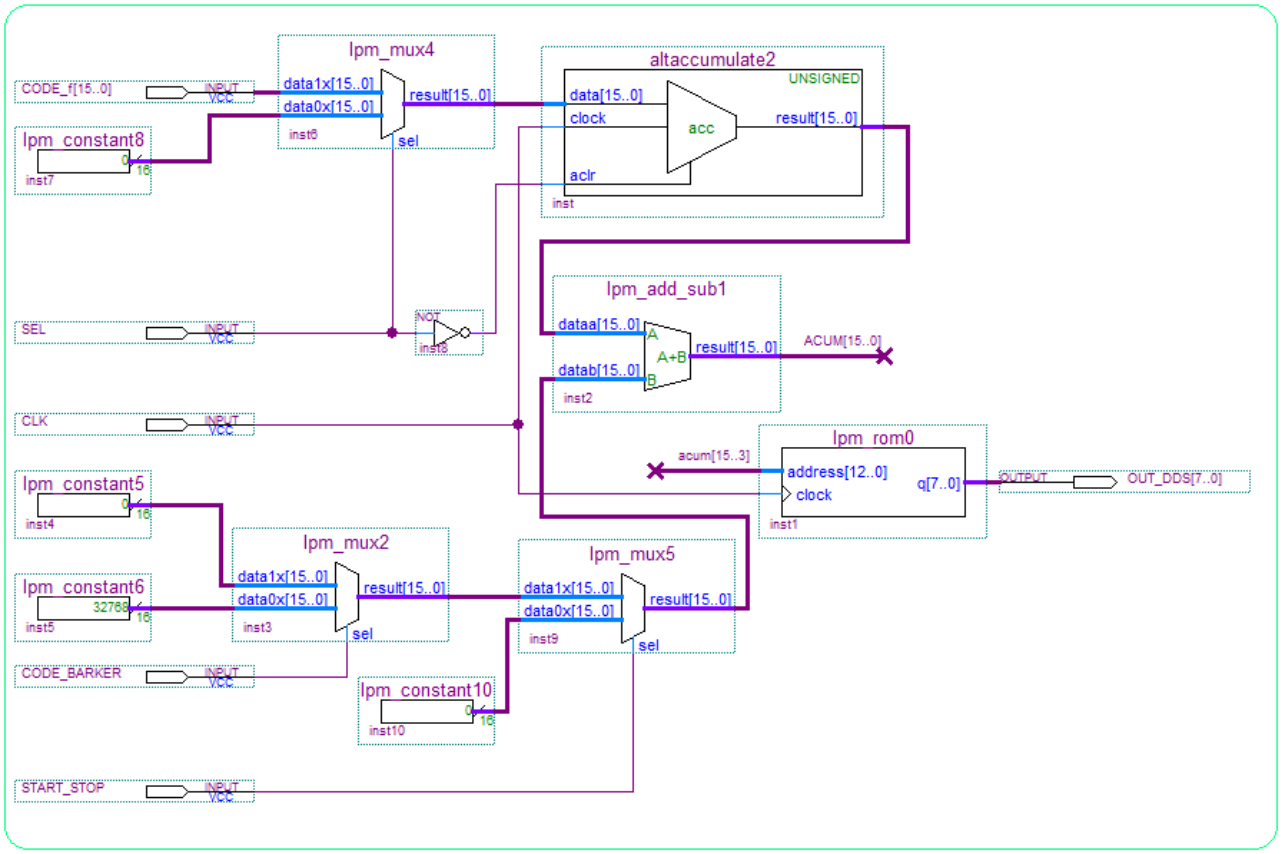

Fig. 18: The functional diagram of the pulse and phase modulator using DDFS

-The pulse modulating signal (Pulse Mod) of repetition period (T) and width (τ) is obtained by DPS using programmable counters for pulse period and pulse width .

-The functional diagram of the pulse width synthesizer using the programming environment QUARTUS II 9.1is shown in the figure.19.

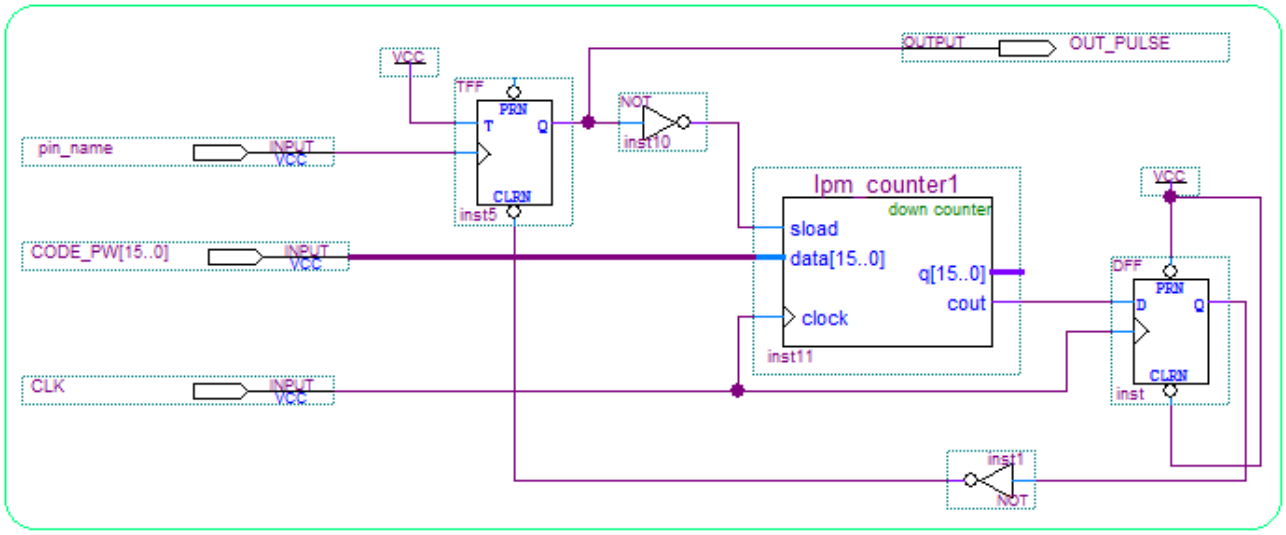

Fig. 19: The functional diagram of the pulse width synthesizer

-The functional diagram of the repetition period synthesizer of the pulses using the programming environment QUARTUS II 9.1 is shown in the figure. 20.

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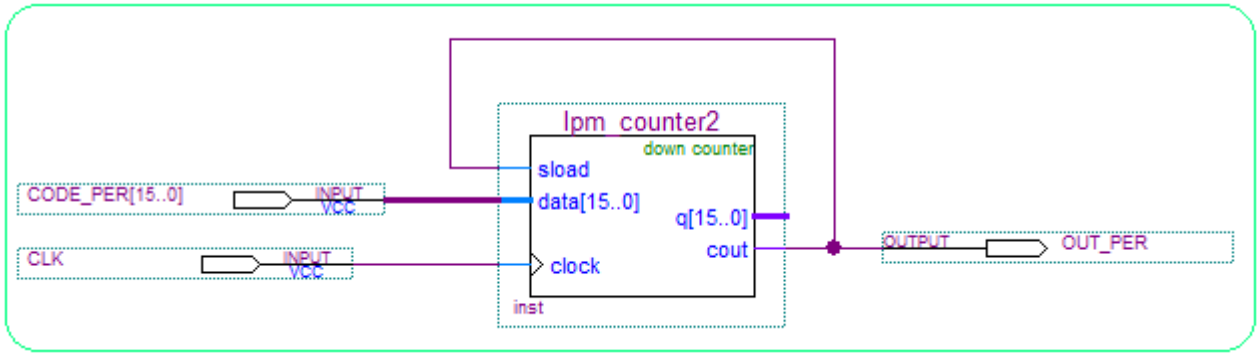

Fig. 20: The functional diagram of the repetition period synthesizer of the pulses

VIII. RESULTS AND CONCLUSION

The results of the practical design for the BPSK modulator for radar signals in time and frequency domains according to the previous application using the FPGA chip placed on education and development board DE1 are shown in figure. 21 in case (N=5),without modulation BPSK and with BPSK modulation , figure. 22 in case (N=7),without modulation BPSK and with BPSK modulation, figure. 23 in case (N=11), without modulation BPSK and with BPSK modulation, and figure. 24 in cases of BPSK according to Barker codes of chips (N=13), these figures are taken from screen of oscilloscope and digital spectrum analyzer[9].

We not from the practical results the identification between the theoretical results and the practical results which indicate the high accuracy of digital synthesizing and modulation operations for signals.

-Using DDFS techniques in radar domain allows implementing digital pulse modulation operations BPSK according to Barker codes with different chips 5, 7, 11, 13 accurately.

-Using DDFS techniques in radar domain allows implementing the digital processing in the radar receiver on high intermediate frequency for BPSK signals according to Barker codes [10].

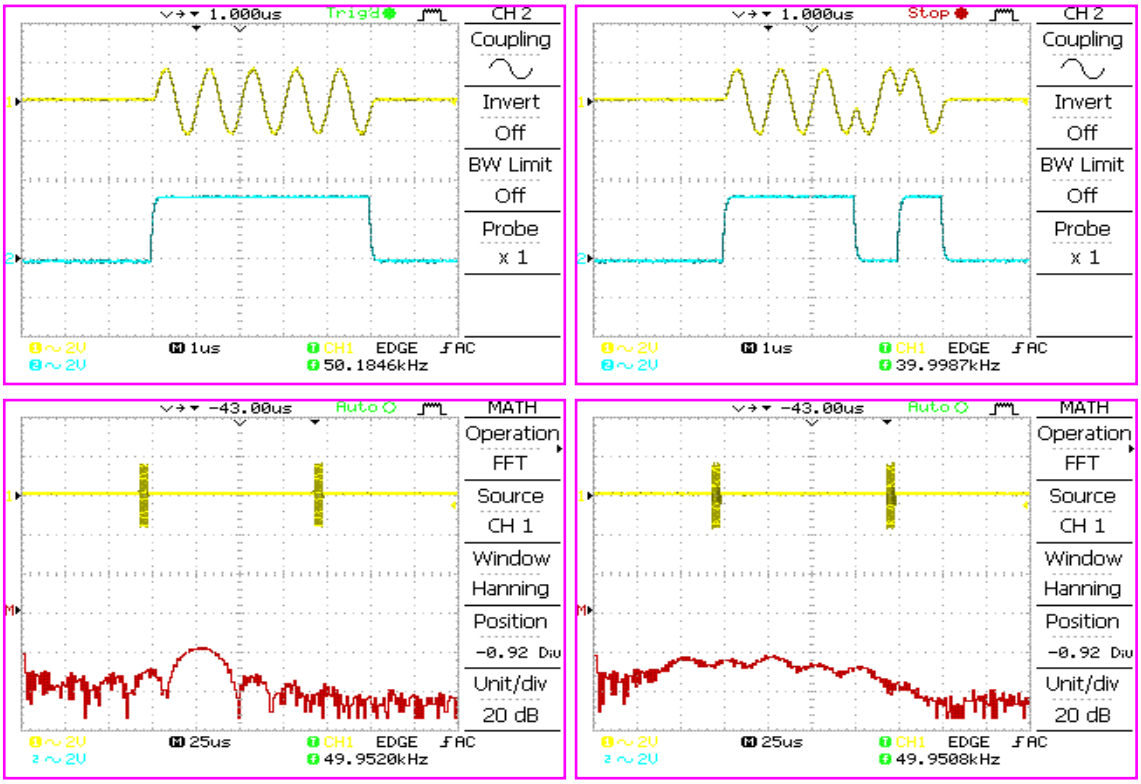

Fig. 21 : Pulse modulation, BPSK signals for N=5 in time and frequency domains

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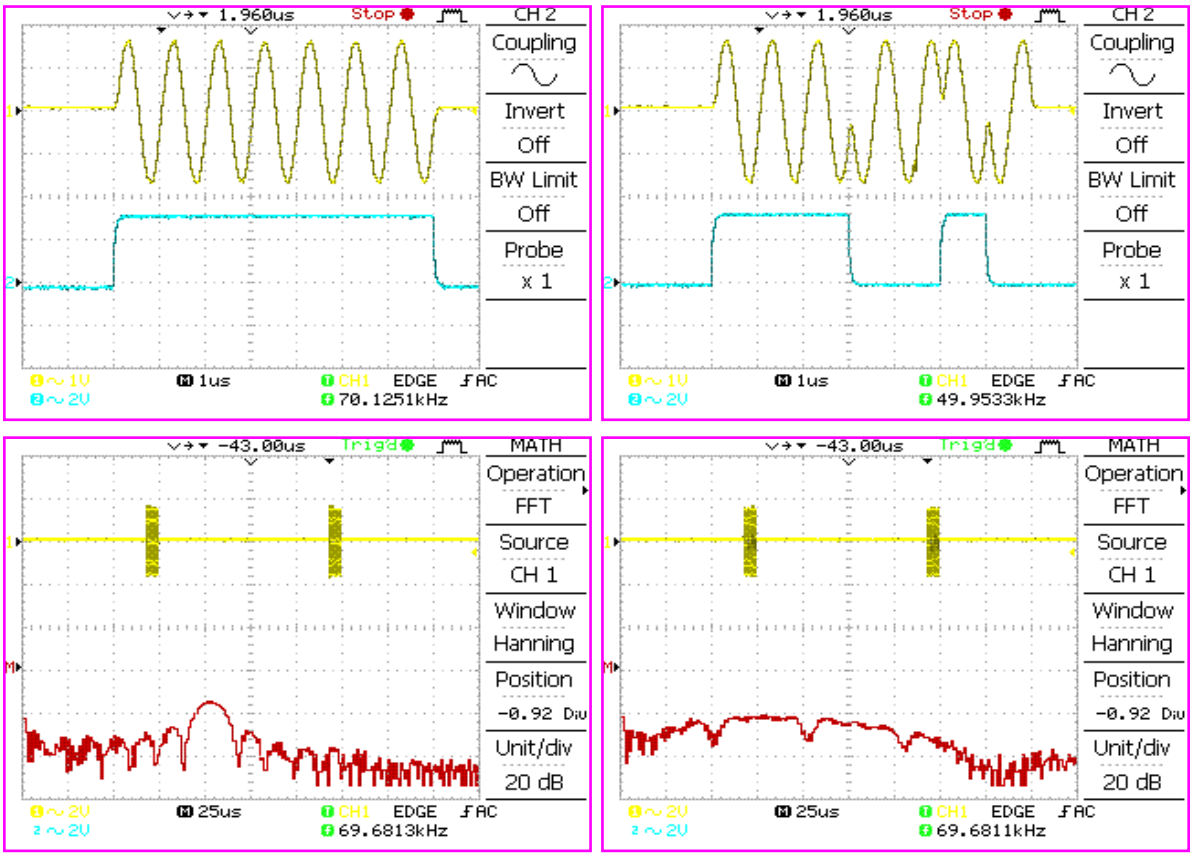

Fig. 22: BPSK signals for N=7 in time and frequency domains

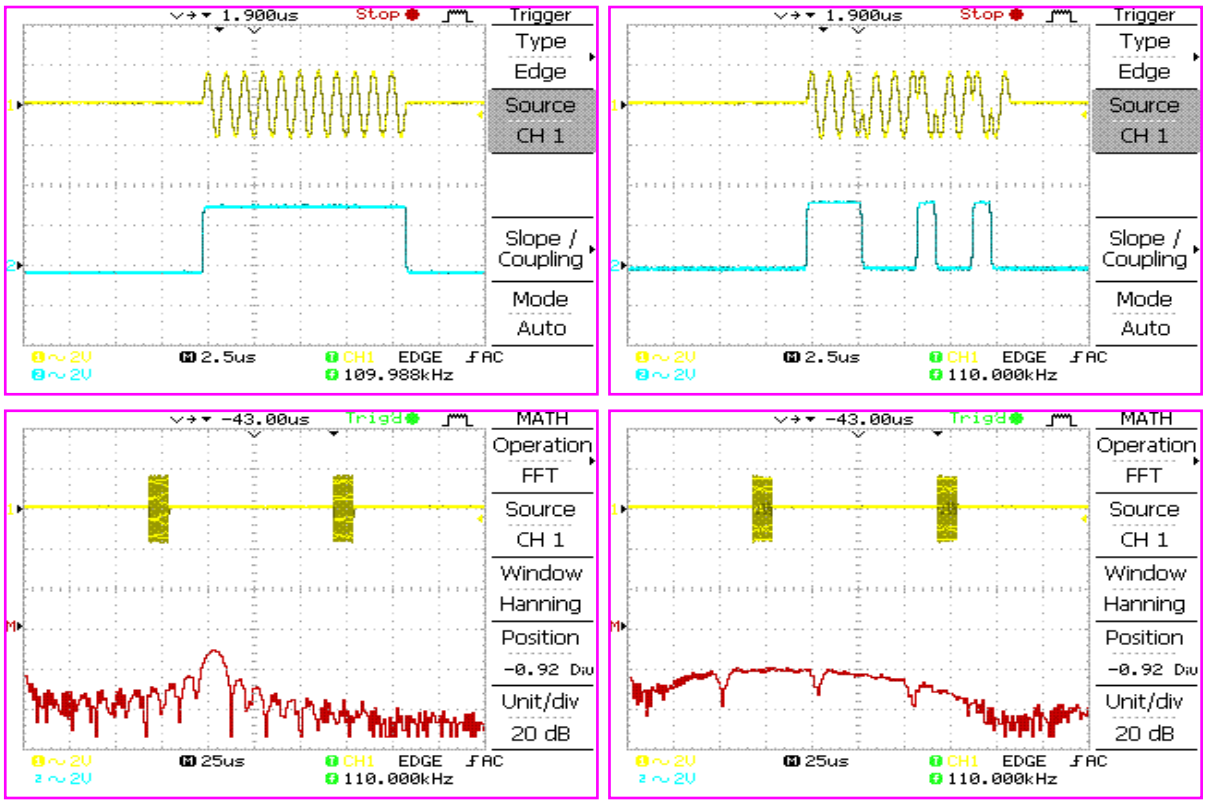

Fig. 23: BPSK signals for N=11 in time and frequency domains

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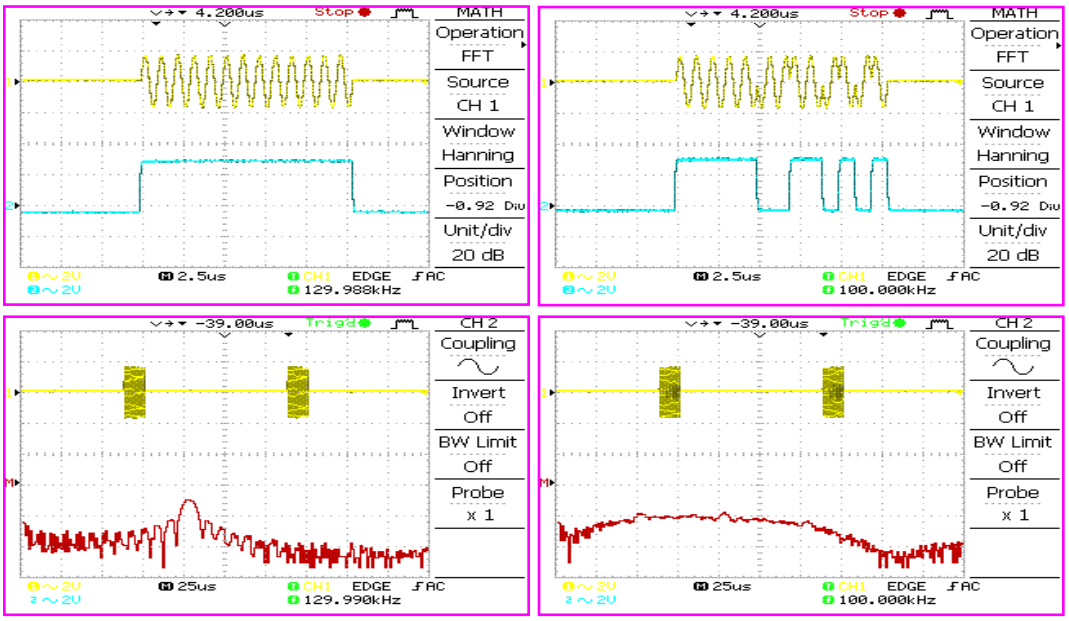

Fig. 24: BPSK signals for N=13 in time and frequency domains

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