International Multidisciplinary Research Journal Reviews (IMRJR)

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 2, Issue 9, September 2025
DOI 10.17148/IMRJR.2025.020902

Design and Implementation of a FIR Digital Hilbert Filter (HF) using FPGA

Dr. Kamal Aboutabikh[1], Dr. Abdul-Aziz Shokyfeh[2], Dr. Amer Garib[3]

Faculty of Informatics Engineering, Ittihad Private University, Damascus- Syria [1,2,3]

Abstract:
The Hilbert Filter (HF) is designed to shift the phase of the input signal by 90 degrees.
The Hilbert Filter is used in many fields, most notably in communication engineering, especially in single side band SSB modulators and demodulators.
In these applications, two components of the audio signal or message signal are generated: the first component is ether the direct in-phase or sinusoidal component, while the second component is shifted by 90 degrees relative to the first. These is achieved using a digital FIR–Type Hilbert Filter.
In this paper, we propose the design and implementation mechanism for FIR digital HF based on the use of Cyclone II EP2C20F484C7 FPGA from ALTERA, placed on education and development board DE-1. The designed filter has the following parameters**:**
-Clock frequency: F_{CLK}=50 MHz.
-Sampling frequency: fsam= 50 MHz.
-Frequency range of the Hilbert filter (HF): (0.05…0.95) x fsam/2 = (1.25 MHz,….,23.75 MHz).
-Type of input signal is: sinusoidal of frequency: finp1=1.25 MHz, finp2=2.5 KHz, finp3=3.75 MHz, finp4=4 MHz.
-The ROM capacity for the stored input signal samples is 8192X9 bits, and their values are positive within the range from (0 to 511).
-Frequency range: (0.001 Hz…25 MHz).
-Frequency Resolution: (0.001 Hz).
-Signal amplitude (5V).
Digital designs using FPGA allow the system to be modified and developed to obtain better results through reprogramming according to the user's desire.

Keywords: Hilbert filter, FIR, DDFS, FPGA.

I. INTRODUCTION

FPGA is considered as one of the distinctive tools for designing digital filters, because it contains a large number of logical elements. It is possible to design digital filters with a high order. Multi-shape windows can also be used to improve specifications of digital filter.

In this paper, we propose a new method to replace floating-point coefficients with integer coefficients, which makes the filtering process parallel and fast, and reduces the memory capacity used to store the coefficients, and approaches the accuracy of the fractional coefficient case.

The coefficients of the designed FIR digital HF h(n) are computed in (MATLAB) environment, and converted to signed values (-511,…,+511) with length (10) bits, then they are used in the filter design program by (VHDL) language, where the digital convolution algorithm of the FIR digital HF is implemented for impulse response samples of length (N=75) as shown in figure (1) , where(Z^{-1}) represents a digital delay line of length (9) bits and a delay time equal to sampling pluses period (Tsam=0.02usec). This digital HF is designed by (VHDL) [1] with (Quartus II9.1) programming environment according to the ideal frequency response shown figure (2).

Reference [2] presents the Design and Implementation of a digital FIR HF with filter length 27 , sampling frequency 140 MHz, Pass band (normalized) : 0.1-0.9.

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 2, Issue 9, September 2025
DOI 10.17148/IMRJR.2025.020902

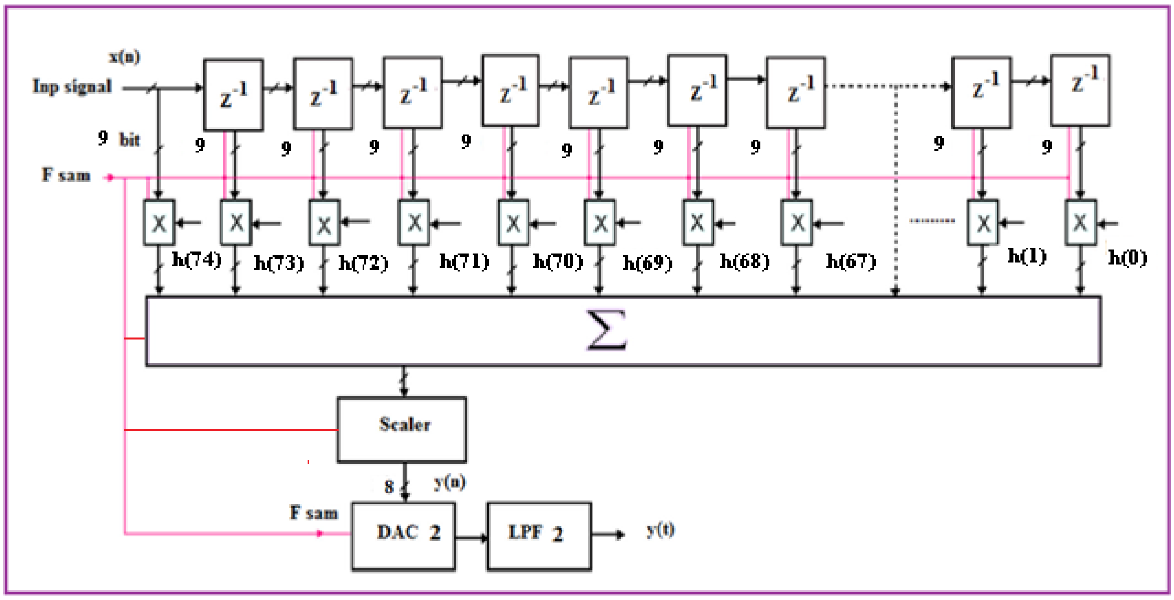

Fig. 1: The block diagram of the FIR digital HF

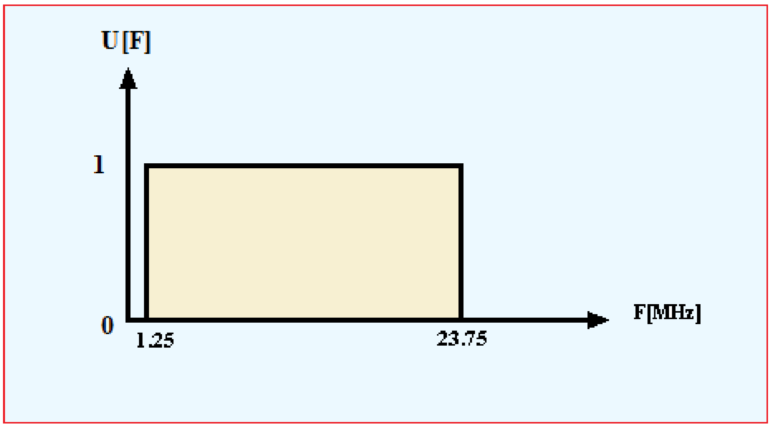

Fig. 2: The ideal frequency response of the digital HF

II. RESERCH IMPORTANCE AND ITS OBJECTIVES

- In this paper, FIR digital HF was designed, implemented and tested based on the use of FPGA, VHDL and Graphical programming language of Quartus II 9.1 design environment.

- Using the digital convolution with mathematical operations (shifting, adding, multiply, division), makes the digital filters design process flexible, accurate and highly efficient.

- Changing the parameters of input signal (frequency), windows type, and filters order explains the difference between digital filters and analog filters.

III. RESERCH MATERIALS AND ITS WAYS

The following tools and software are used to design, and test digital filters of different types (LPF, HPF, BPF, HF), different window types, and different values of input signals:
-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].
-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment.
-Design Environment MATLAB.
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [4] is shown in figure (3).

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 2, Issue 9, September 2025
DOI 10.17148/IMRJR.2025.020902

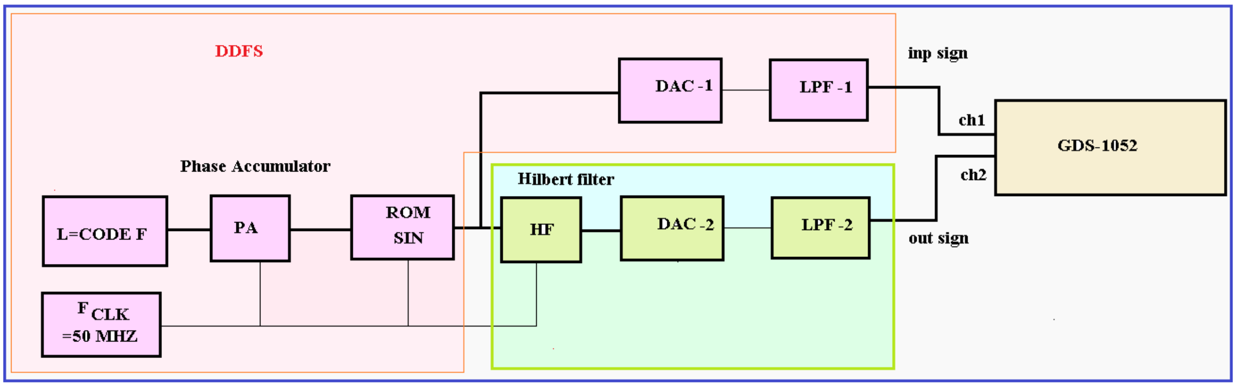

Fig (3): Block diagram of the laboratory experiment platform

IV. DESIGN OF THE DDFS USIGN QUARTUS II 9.1

The designed DDFS has the following parameters:
-The frequency step i : $\delta f = 0.001\ Hz\ , and\ f_{clk} = 50\ MHz$.
-The input signal is sinusoidal of frequency finp1=1.25 MHz , finp2=2.5 MHz, finp3=3.75 MHz, finp4=4 MHz and fsam= 50 MHz.
-The ROM capacity for the stored signal samples 8192X8 bits, and their values are positive within the range from 0 to 255.
-The number of the accumulator bits is computed from the following mathematical relation [5]:

$$\delta f = \frac{f_{clk}}{2^n} \quad (1)$$

$$\delta f = \frac{f_{clk}}{2^n} \Longrightarrow 2^n = \frac{f_{clk}}{\delta f} = \frac{50\ X\ 10^6}{0.001} \Longrightarrow n = 32 \text{ bits}$$

-The frequency range for the DDFS is computed from the following mathematical relation:

$$\Delta f = 0 \ldots\ldots \frac{f_{clk}}{2} = 0 \ldots .25\ MHz$$

- The frequency code is calculated according the following relation [6]:

$$Code\ f = L = \frac{f\ X\ 2^{\text{n}}}{f_{clk}} \quad (2)$$

So to synthesize seven input signals of frequencies finp1=1.25 MHz, finp2=2.5 MHz, finp3=3.75 MHz, finp4=4 MHz and fsam= 50 MHz, the frequency code of each one will be:

$$Code\ f_{inp1} = L_{inp1} = \frac{f_{inp1}\ X\ 2^{\text{n}}}{f_{clk}} = \frac{1.25\ X\ 2^{32}}{50} = 107374182$$

$$Code\ f_{inp2} = L_{inp2} = \frac{f_{inp2}\ X\ 2^{\text{n}}}{f_{clk}} = \frac{2.5X\ 2^{32}}{50} = 214748365$$

$$Code\ f_{inp3} = L_{inp3} = \frac{f_{inp3}\ X\ \ 2^{\text{n}}}{f_{clk}} = \frac{3.75X\ 2^{32}}{50} = 322122547$$

$$Code\ f_{inp4} = L_{inp4} = \frac{f_{inp4}\ X\ 2^{\text{n}}}{f_{clk}} = \frac{4\ X\ 2^{32}}{50} = 343597384$$

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 2, Issue 9, September 2025
DOI 10.17148/IMRJR.2025.020902

V. FILTERING ALGORITHM

The FIR digital HF output signal can be represented according to the following convolution relationship [7]:

$$y(n) = h(n) * x(n) = \sum_{k=0}^{N-1} h(k).x(n-k) \tag{3}$$

Where: *x(n)* is the input signal samples in digital form.
N is number of samples for impulse response of the filter.
n is the sample number for input and output signals.
h(n) is the impulse response samples of the digital filter, and it is given for HF according to the following relationship [8]:

$$a_n = h(n) = 0\,, \quad for\ n = \frac{N-1}{2} \tag{4}$$

$$a_n = h(n) = \frac{2}{\pi\left(n - \frac{N-1}{2}\right)}\ , \quad for\ n \neq \frac{N-1}{2} \tag{5}$$

Where:

$$n = 0, \ldots\ldots.., N-1$$

$$-\frac{(N-1)}{2} \leq k \leq \frac{(N-1)}{2} \tag{6}$$

For N=74:

$$-\frac{(N-1)}{2} \leq k \leq \frac{(N-1)}{2} \Rightarrow -37 \leq k \leq 37$$

$$h_{nor}(k) = \frac{h(k)}{h_{MAX}(k)} \tag{7}$$

$$h_{int}(k) = INT[511 * h_{nor}(k)] \tag{8}$$

Where:
$h_{nor}(k)$ Relative value, $\{h_{MAX}(k) = 0.635489130396366 34\}$ Maximum value, $h_{int}(k)$ Integer value.
The values of $h(k)$ are calculated using the MATLAB environment, Toolboxes-Filter Design-Filter Design & Analysis Tool (fdatool), and then $h_{nor}(k)$, $h_{MAX}(k)$, $h_{int}(k)$ are recalculated according to the relationships (5), (6) and recorded in table (1).

Table (1)

n	k=n-37	h(n)= h(k)	$h_{nor}(n) = h(n)/ h_{max}(m)$	$h_{int}(n)$= INT[511* h_{nor}(n)]
0	-37	-0.00085722161432619638	-0.0013489162494274786151698664 0806	-1
1	-36	-0.00000028010269944596541	0	0
2	-35	-0.0010916337758430303	-0.0017177851258638493104593413 1163	-1
3	-34	-0.000000015841102337986877	0	0
4	-33	-0.0017581988353015422	-0.0027666859293170302130378060 6726	-1
5	-32	0.00000000856410895615 68389	0	0
6	-31	-0.0026671831160352123	-0.0041970554466787508919670716 5263	-2
7	-30	0.0000000261406263240835 72	0	0
8	-29	-0.003872715335008315	-0.0060940701418336309264300442 4132	-3
9	-28	0.000000399446112468098 6	0	0

10	-27	-0.0054371155618995158	-0.00855579631788239419247891598632	-4
11	-26	0.00000047431954930167653	0	0
12	-25	-0.0074329842736405097	-0.0116964774346406519153819288539	-6
13	-24	0.0000005900457736337043	0	0
14	-23	-0.0099478826014544122	-0.01565389890343165049088531735353	-8
15	-22	0.00000077859709092365859	0	0
16	-21	-0.013091507958881352	-0.02060067959103554773468515997198	-11
17	-20	0.0000010373656331214363	0	0
18	-19	-0.017008408094065647	-0.02676427853841841145730776679383	-14
19	-18	0.000001346800708639675	0	0
20	-17	-0.021901579618296224	-0.03446412939374085465618667392699	-18
21	-16	0.0000010325321715708568	0	0
22	-15	-0.028070461972611815	-0.04417142737768582760452703705966	-23
23	-14	0.0000013464845129226386	0	0
24	-13	-0.035995441657959981	-0.05664210438266498342142393698393	-29
25	-12	0.0000009660823315594783	0	0
26	-11	-0.046499985621520246	-0.07317196061641108445056958648671	-37
27	-10	0.00000097883365360895724	0	0
28	-9	-0.061149169948382542	-0.09622378577937701658198982012057	-49
29	-8	0.0000010088303849582175	0	0
30	-7	-0.083310408451043649	-0.13109651206635336835028740497941	-67
31	-6	0.00000049433960731670718	0	0
32	-5	-0.12177175554271613	-0.19161894313875176878859414831649	-98
33	-4	0.00000048871627675888587	0	0
34	-3	-0.2088350089307992	-0.32862089836303720453618294297837	-168
35	-2	0.00000041488564331517477	0	0
36	-1	-0.63548913039636634	-1	-511
37	**0**	**0**	**0**	**0**
38	1	0.63548913039636634	1	511
39	2	-0.00000041488564331517477	0	0
40	3	0.2088350089307992	0.32862089836303720453618294297837	168
41	4	-0.00000048871627675888587	0	0
42	5	0.12177175554271613	0.19161894313875176878859414831649	98
43	6	-0.00000049433960731670718	0	0
44	7	0.083310408451043649	0.13109651206635336835028740497941	67
45	8	-0.0000010088303849582175	0	0
46	9	0.061149169948382542	0.09622378577937701658198982012057	49
47	10	-0.00000097883365360895724	0	0
48	11	0.046499985621520246	0.07317196061641108445056958648671	37
49	12	-0.0000009660823315594783	0	0
50	13	0.035995441657959981	0.05664210438266498342142393698393	29
51	14	-0.0000013464845129226386	0	0
52	15	0.028070461972611815	0.04417142737768582760452703705966	23
53	16	-0.0000010325321715708568	0	0
54	17	0.021901579618296224	0.03446412939374085465618667392699	18
55	18	-0.000001346800708639675	0	0

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 2, Issue 9, September 2025
DOI 10.17148/IMRJR.2025.020902

56	19	0.017008408094065647	0.02676427853841841145730776679383	14
57	20	-0.0000010373656331214363	0	0
58	21	0.013091507958881352	0.02060067959103554773468515997198	11
59	22	-0.00000077859709092365859	0	0
60	23	0.0099478826014544122	0.01565389890343165049088531735353	8
61	24	-0.0000005900457736337043	0	0
62	25	0.0074329842736405097	0.0116964774346406519153819288539	6
63	26	-0.00000047431954930167653	0	0
64	27	0.0054371155618995158	0.00855579631788239419247891598632	4
65	28	-0.0000003994461124680986	0	0
66	29	0.003872715335008315	0.00609407014183363092643004424132	3
67	30	-0.00000026140626324083572	0	0
68	31	0.0026671831160352123	0.00419705544667875089196707165263	2
69	32	-0.000000085641089561568389	0	0
70	33	0.0017581988353015422	0.00276668592931703021303780606726	1
71	34	0.00000015841102337986877	0	0
72	35	0.0010916337758430303	0.00171778512586384931045934131163	1
73	36	0.00000028010269944596541	0	0
74	37	0.00085722161432619638	0.00134891624942747861516986640806	1

VI. DESIGN OF THE DIGITAL HILBERT FILTER USING MATLAB

The FIR digital Hilbert filter (HF) was designed using MATLAB and VHDL with the following parameters [9]:
-Type of filter : HF.
- Filter structure: Direct form - FIR
-Filter order: 74.
-Filter length: 75.
-Sampling frequency: 50MHz.
-Frequencies of input signals: finp1=1.25 MHz, finp2=2.5 MHz, finp3=3.75 MHz, finp4=4 MHz.
-Cut-off frequency of HF: fcut1=1.25 MHz, fcut2=23.75 MHz.
-Window type: Rectangular.
-Word length for input signal: 9 bits and for filter coefficients: 10 bits
The specification and magnitude response of a digital filter designed in MATLAB is shown in figure (4), impulse response is shown in figure (5) and magnitude (dB) and phase response is shown in figure (6).

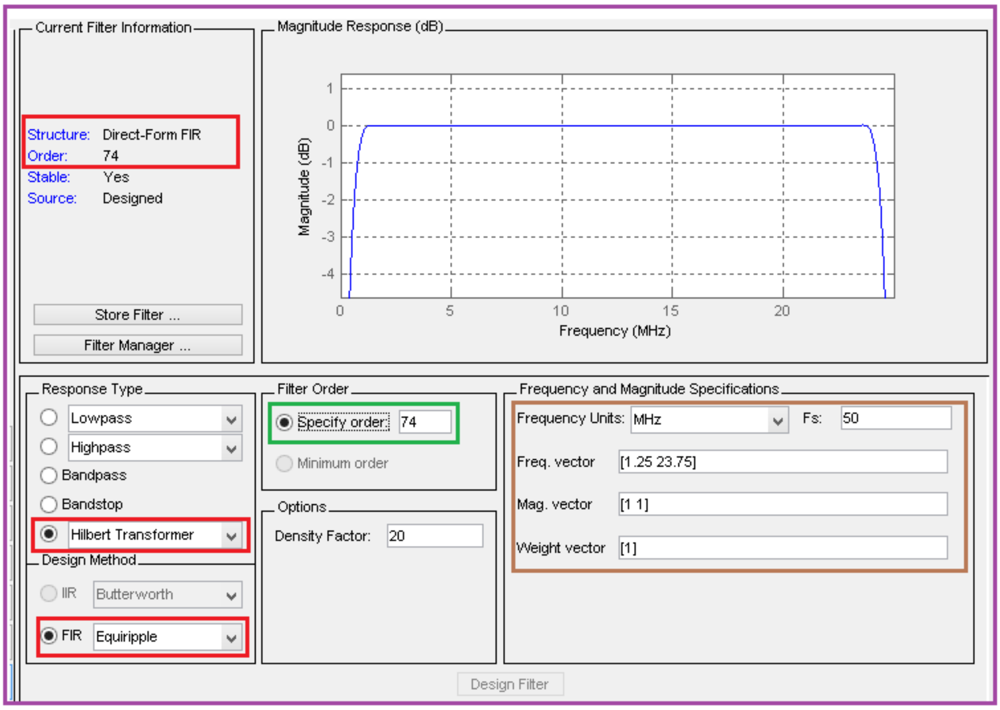

Fig (4): The specification and magnitude response of a digital Hilbert filter designed in MATLAB

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 2, Issue 9, September 2025
DOI 10.17148/IMRJR.2025.020902

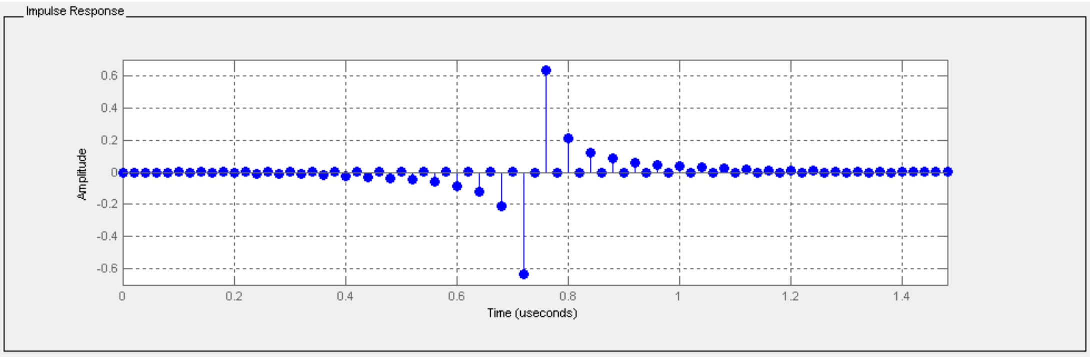

Fig (5): The impulse response of a digital Hilbert filter designed in MATLAB

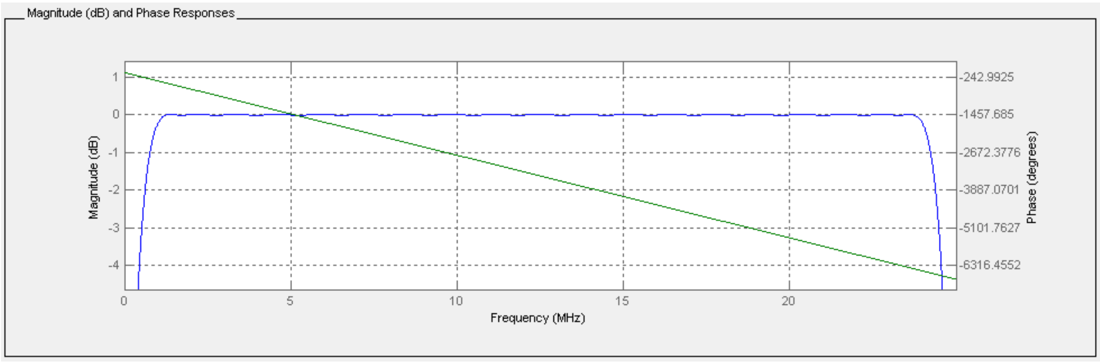

Fig (6): The magnitude and phase response of a digital Hilbert filter designed in MATLAB

The block diagram of the digital HF designed in (Quartus II9.1) environment is shown in figure (7).

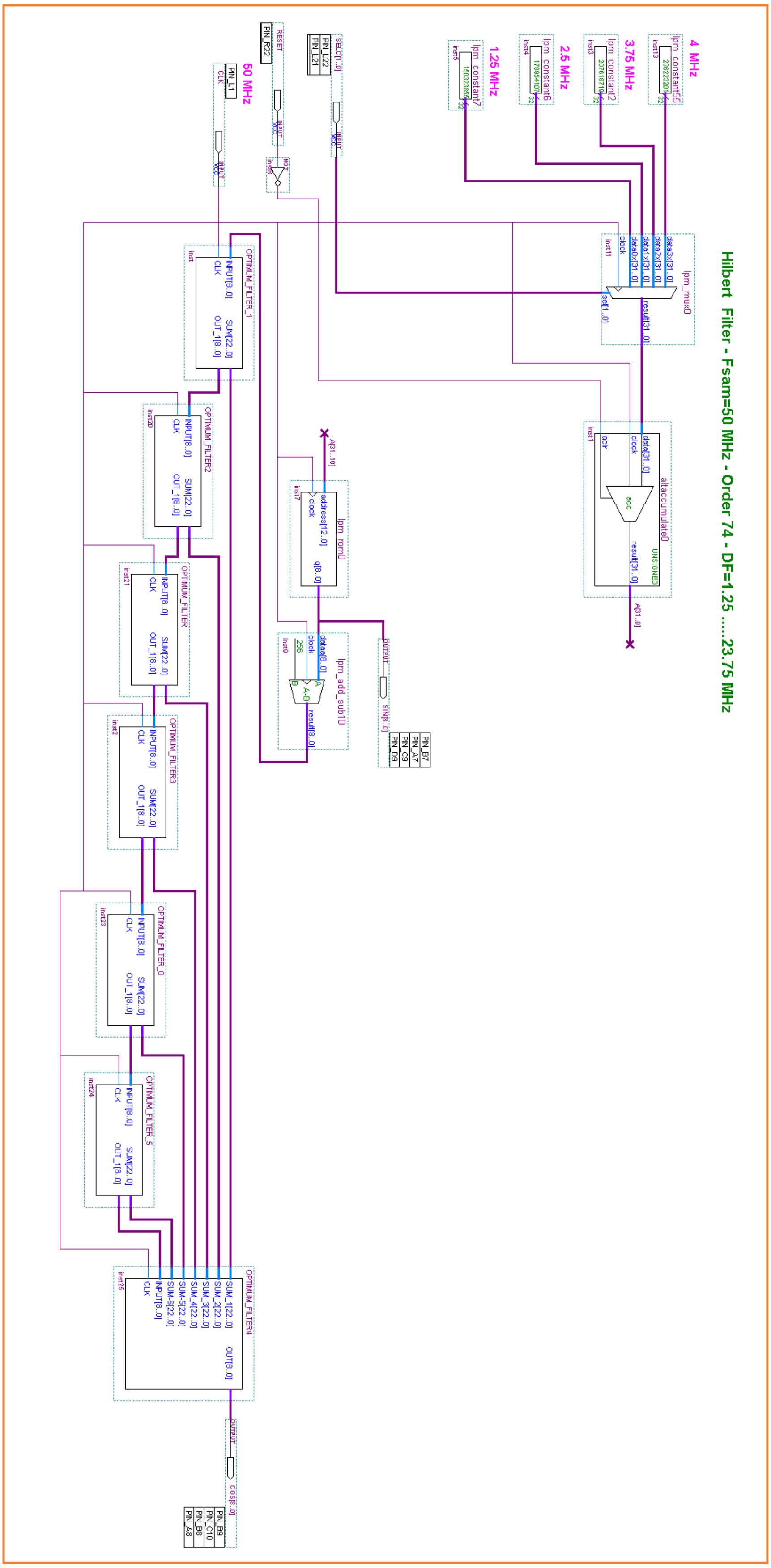

Fig (7): The block diagram of a digital HF in (Quartus II9.1)

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 2, Issue 9, September 2025
DOI 10.17148/IMRJR.2025.020902

VII. RESULTS OF DESIGN

The results of the practical design of the digital HF for different cases in time domain are shown in figure (7), figure (8), figure (9) and in figure (10).

Figure (7) shows the input signal (CHANNEL 1) and output signal (CHANNEL 2) of a HF for a signal frequency finp1=1.25 MHz, we notice that the phase shift between the input signal and output signal is approximately 90 degrees.

Figure (8) shows the input signal (CHANNEL 1) and output signal (CHANNEL 2) of a HF for a signal frequency finp2=2.50 MHz, we notice that the phase shift between the input signal and output signal is approximately 90 degrees. Figure (9) shows the input signal (CHANNEL 1) and output signal (CHANNEL 2) of a HF for a signal frequency finp3=3.75 MHz, we notice that the phase shift between the input signal and output signal is approximately 90 degrees. Figure (10) shows the input signal (CHANNEL 1) and output signal (CHANNEL 2) of a HF for a signal frequency finp4=4 MHz, we notice that the phase shift between the input signal and output signal is approximately 90 degrees. The results (figure (7), figure (8), figure (9) and figure (10)) of the practical design of the digital HF are taken from the screen of digital oscilloscope GDS-1052.
From these results we notice that the phase shift between the input signal and output signal is approximately 90 degrees, and we also notice from these results the identification between the theoretical results and the practical results, which indicate the high accuracy of digital synthesizing and filtering operations.

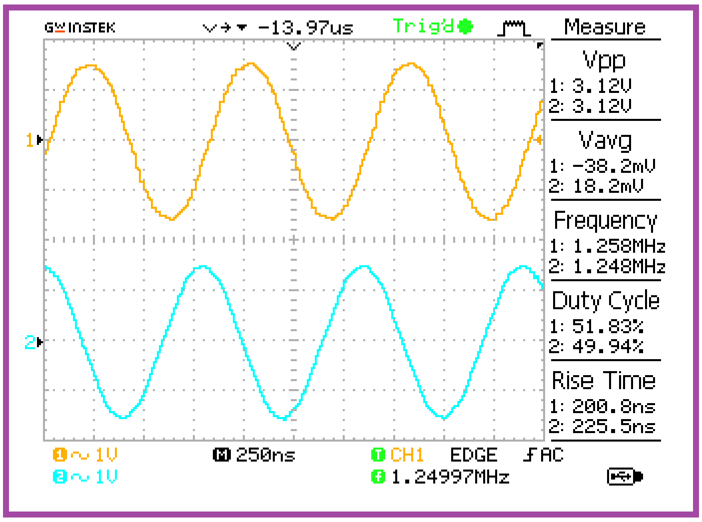

Fig. (7): The input and output signals of HF for finp2=1.25 MHz in time domain.

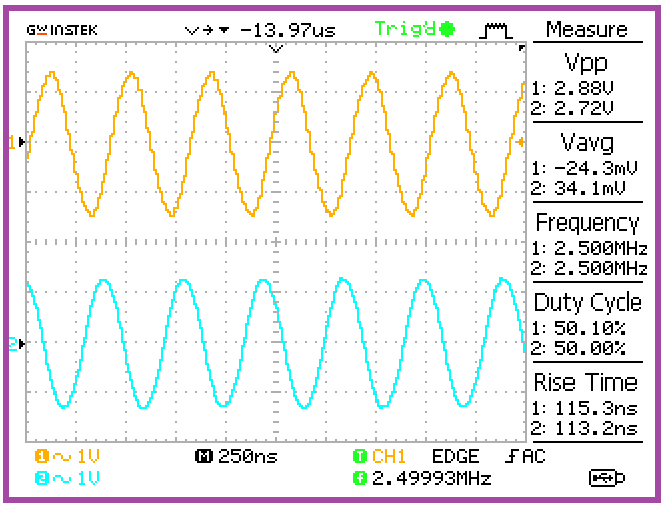

Fig. (8): The input and output signals of HF for finp2=2.50 MHz in time domain.

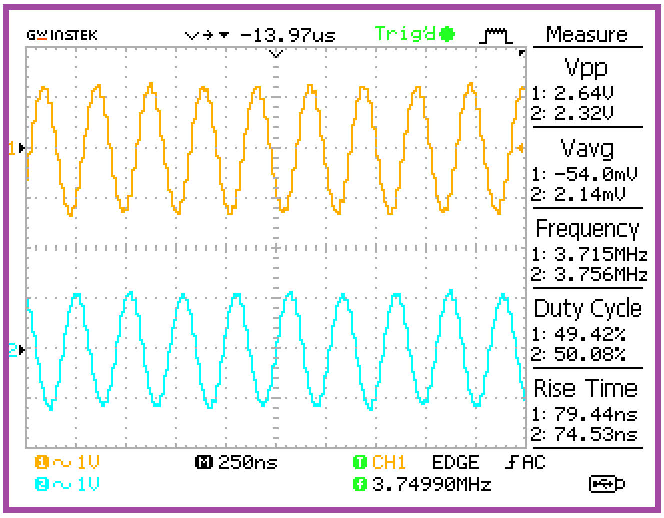

Fig. (9): The input and output signals of HF for finp3=3.75 MHz in time domain.

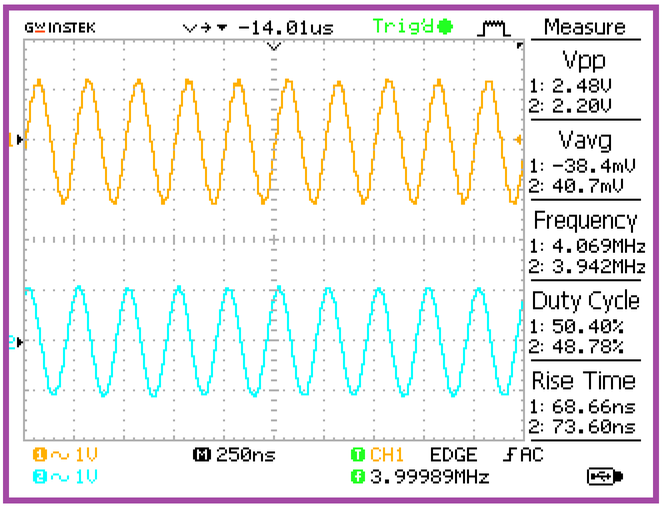

Fig. (10): The input and output signals of HF for finp4=4 MHz in time domain.

VIII. DISCUSSION AND CONCLUSION

-Using digital filtering techniques in communication domain allows implementing different filters (LPF, HPF, BPF, SBF, HF etc) with high accuracy and speed, and with the ability of changing parameters of signals in wide range.
-The use of a Hilbert filter in the field of communications allows for achieving a 90- degrees phase shift between the frequency components of the input signal and the output signal.
-We note from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital filtering for signals.
-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).
-The most important feature of this paper is the ability to change the frequency of the input signals within a wide frequency range.
-The performance or specifications of a digital Hilbert filter can be improved by:

- Increasing the filter order N up to 150.
- Increase the number of input signal bits up to 16 bits and the number of filter coefficients bits up to 16 bits.
- Changing the window type.

-To obtain a phase shift resolution of 90 degrees, a band-pass filter can be used before the Hilbert filter to restrict the wide frequency range.

REFERENCES

[1]. Volnei A. Pedroni, “Circuit Design With VHDL”, MIT Press Cambridge, Massa- chusetts London, England (2004) 364.

[2]. Duraiswamy et al. EURASIP Journal on Advances in Signal Processing 2011, 2011:32, http://asp.eurasipjournals.com/content/2011/1/32. Efficient implementation of 90° phase shifter in FPGA

[3]. Emmanuel S. Kolawole, Warsame H. Ali, Penrose Cofie, John Fuller, C. Tolliver, Pamela Obiomon “Design and Implementation of Low-Pass, High-Pass and Band-Pass Finite Impulse Response (FIR) Filters Using FPGA “, Circuits and Systems, 2015, 6, 30-48 Published Online February 2015 in SciRes. http://www.scirp.org/journal/cs http://dx.doi.org/10.4236/cs.2015.62004.

[4]. ALTERA, CORPORATION," Cyclone II Device Family Data Sheet"; 2005.

[5]. Dr. Kamal Aboutabikh, Dr. Abdul-Aziz Shokyfeh, Dr. Amer Garib, “Design and Implementation of a Digital Quadrature Amplitude Modulator QAM-16 using FPGA”, International Multidisciplinary Research Journal Reviews, Volume 1, Issue, 2, October 2024.

[6]. GOLDBERG B. “Digital Frequency Synthesis Demystified”, LLH Technology Publishing, united states, 334,1999-.

[7]. ANALOG DIVISE, “A Technical Tutorial on Digital Signal Synthesis”.

[8]. Steve Winder, “Analog and Digital Filter Design”, second edition, Elsevier Science, USA (2002) 450.

[9]. Manoj Sharma, Hemant Dalal, “Designing and implementation of digital filter for power line interference suppression”, Int.J.Sci.Eng. Technol.Res.3(6) (2014)1831–1836, June.

[10]. ⟨http://www.mathworks.com/matlabcentral/fileexchange/10858-ecg-simulation- using-matlab⟩.

BIOGRAPHY

Dr. Kamal Aboutabikh: Holds a PhD in communication engineering in 1988 from the USSR, university of communication in Leningrad. Holds assistant professor degree in 2009 from Aleppo university.
Lecturer at Department of Biomedical Engineering, Al Andalus University For Medical Sciences-Syria. Lecturer at Tishreen University-Syria, and Corduba Private University- Syria. Former Lecturer at Kassala University-Sudan and Ittihad Private University- Syria.
Published a lot of researches in the field of digital communication, and digital signal processing in the university’s journals of Syria and in the European and Indian journals.
Working in the field of programming FPGA by using VHDL, and designing Digital Filters.

Dr. Abdul-Aziz Shokyfeh holds a PhD in telecom engineering in 2017 from Damascus Syria, Faculty of Mechanical and Electrical Engineering Telecommunication and electronic department.
Lecture at Electric engineering, computer engineering, control and automation engineering, telecom and electronic engineering at Damascus University.
Dean of IT college at Ittehad Private University, from 2023 till now.
Publish a lot of research in field of antenna in Syrian and European journals. Working in field of PBXs, Network, low current system and solution.

Dr. Amer Garib holds a PhD in communication engineering in 1994 from the USSR, university of communication in Leningrad. Lecturer at Department of Faculty of Informatics Engineering, Ittihad Private University- Syria.
Publish a lot of research in the field of digital communication in the universities of Syria and in the Indian journals. Working in the field of Digital Communication System.