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Design and Implementation of a Digital Laboratory Experiment to Obtain Lissajous Figures Using FPGA

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Abstract: In this paper, a two-output direct digital frequency synthesizer (DDFS) is designed to generate two sinusoidal signals: one with a reference signal with a zero initial phase, and the other with a phase control within a range of 0 to 360 degrees at a 45-degree angle. The first signal has two frequencies of 1 MHz or 2 MHz, while the second signal has three frequencies of 1 MHz , 2 MHz or 3 MHz .
The purpose of this design is to obtain Lissajous Figures for the frequency ratio between the first signal and the second signal is (1/1, 1/2, 1/3, 2/3), and the initial phase values of the second signal for each ratio takes the values (0, 45, 90, 135, 180, 225, 270, 315) degrees.
Also, we discuss a practical mechanism of a dual-output direct digital frequency synthesizer (DODDFS) using Cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1 with the following parameters:
-Output waveforms: sinusoidal.
-Frequency range: (3Hz…..10 MHz).
-Frequency Resolution (3Hz).
-Signal amplitude (5V).
-With Reset of the DODDFS.
-Frequency of the generated signal for all types signals: (1 MHz, 2 MHz, 3 MHz).
-Phase shifts: (0,45,90,135,180,225,270,315) degrees.

Keywords: Lissajous Figures, DDFS, DODDFS, FPGA.

I. INTRODUCTION

The educational laboratory experiments are considered as an effective tool for learning and understanding the theoretical engineering sciences. They build a solid basis to develop the theoretical basics of engineering sciences, and to emerge towards science research especially in the field of electronic, communication, and radar engineering. Designing of educational laboratory experiments by software packages using FPGA has the following features:

- All connections between electronic elements and data buses and entries and outputs of the experiment are programmatic, and could be modified during the phase of designing and simulation and execution. It means no wiring, no routing, no burning or corruption of the electronic circuit in the phase of building.
- All experiments are available for modifying and updating through adding or deleting or changing in programmatic way.
- Every experiment has its own software package which is injected into the FPGA at the beginning of execution, and is deleted at the end of execution. It means that there is One Electronic Hardware for all experiments, which may count to hundreds, through various software packages. For example, traditionally we need 50 boards for 50 experiments, every board is specified for one experiment with its own connections, which considered expensive, complex, low reliable because of multifunction's resulted of manually wiring. Besides to the long time expired to assemble the experiment before executing.
- Performing researches and practical studies in various fields such as electronic, communication, radar, and medical engineering.
- Most companies that produce laboratory software packages make them closed without the ability to make any modification or addition to it, because they make a financial profit from it.

II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

The aim of the research is to design a digital laboratory experiment to obtain high-resolution Lissajous figures. This can be achieved by using a dual-output direct digital frequency synthesizer for different values of the frequency's ratio and different values of the initial phase shift between the two signals.

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The accuracy of frequency and resolution of the initial phase shift for DODDFS is achieved by increasing the number of phase accumulator bits, and by increasing the memory capacity of the sinusoidal signal samples stored in the memories (ROM's).
These experiments become more efficient if they were built using tools of high processing and arithmetic speed such as processors and FPGA' s (Field Programmable Gate Arrays) and FPAA' s (Filed Programmable Analog Arrays).

III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the DODDFS for different types of signals, the following tools and software are used:
- Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [1].
- DODDFS which is considered as highly accuracy techniques in Sinusoidal and Cosine signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment [2].
- Design Environment MATLAB R2008a.
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.

IV. BLOCK DIAGRAM OF THE DUAL-OUTPUT DIRECT DIGITAL FREQUENCY SYNTHESIZER (DODDFS) WITH CONTROLLED PHASE SHIFT

This synthesizer is used to digitally generate tow sin signals with phase difference in the range $(\Delta\varphi = 0 \ldots .2\pi)$ so we can display different Lissajous figures.

The characteristics of DODDFS:
-The frequency of DODDFS is computed according the following equations [3]:

$$x = sin(2\pi f_x t)\ , \qquad y = sin\left(2\pi f_y t + \Delta\varphi\right)$$

$$f_x = \frac{F_{CLK}.L_{fx}}{2^n} \quad \Rightarrow L_{fx} = \frac{2^n\ .f_x}{F_{CLK}} \qquad (1)$$

$$f_y = \frac{F_{CLK}.L_{fy}}{2^n} \quad \Rightarrow L_{fy} = \frac{2^n\ .f_y}{F_{CLK}} \qquad (2)$$

-The phase shift is computed according the following equation [3]:

$$\Delta\varphi = \frac{2\pi.X_\varphi}{2^n} \quad \Rightarrow X_\varphi = \frac{2^n\ .\Delta\varphi}{2\pi} \qquad (3)$$

Where: $X_\varphi = (0, \ldots., 2^n)$ code of phase shift.

$$For\ n = 24\ bits\ , \Delta\varphi = 0\ \ then: X_\varphi = \frac{2^n\ .\Delta\varphi}{2\pi} = \frac{2^{24} * 0}{2\pi} = 0$$

$$For\ n = 24\ bits\ , \Delta\varphi = \frac{\pi}{4}\ \ then: X_\varphi = \frac{2^n\ .\Delta\varphi}{2\pi} = \frac{2^{24} * \frac{\pi}{4}}{2\pi} = 2^{21} = 2097152$$

-The phase resolution is the value of $(\Delta\varphi)$ for $\left(X_\varphi = 1\right)$ then:

$$\delta\varphi = \frac{2\pi.X_\varphi}{2^n} = \frac{2\pi * 1}{2^{24}} = 3.75 * 10^{-7}\ Rad$$

Or:

$$\delta\varphi = \frac{360.X_\varphi}{2^n} = \frac{360 * 1}{2^{24}} = 0.0002\ \ Deg$$

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$For\ f_x = f_y = 1\ MHz$ then:

$$L_{fx} = L_{fy} = \frac{2^n\ .f_x}{F_{CLK}} = \frac{2^{24}\ .1}{50} = 335544$$

$For\ f_x = 1\ MHz\ , f_y = 2\ MHz\ \left(\frac{f_x}{f_y} = \frac{1}{2}\right)$ then:

$$L_{fx} = \frac{2^n\ .f_x}{F_{CLK}} = \frac{2^{24}\ X\ 1}{50} = 335544$$

$$L_{fy} = \frac{2^n\ .f_y}{F_{CLK}} = \frac{2^{24}\ X\ 2}{50} = 671089$$

$For\ f_x = 1\ MHz\ , f_y = 3\ MHz\ \left(\frac{f_x}{f_y} = \frac{1}{3}\right)$ then:

$$L_{fx} = \frac{2^n\ .f_x}{F_{CLK}} = \frac{2^{24}\ X\ 1}{50} = 335544$$

$$L_{fy} = \frac{2^n\ .f_y}{F_{CLK}} = \frac{2^{24}\ X\ 3}{50} = 1006633$$

$For\ f_x = 2\ MHz\ , f_y = 3\ MHz\ \left(\frac{f_x}{f_y} = \frac{2}{3}\right)$ then:

$$L_{fx} = \frac{2^n\ .f_x}{F_{CLK}} = \frac{2^{24}\ X\ 2}{50} = 671089$$

$$L_{fy} = \frac{2^n\ .f_y}{F_{CLK}} = \frac{2^{24}\ X\ 3}{50} = 1006633$$

-Frequency Resolution:
for L=1 then:

$$\delta f = \frac{F_{CLK}.L}{2^n} = \frac{50\text{x}10^6}{2^{24}} = 3\ Hz \qquad (4)$$

f_x (MHz)	1	1	1	2
f_y (MHz)	1	2	3	3
$f_x/\ f_y$	1/1	1/2	1/3	2/3

-Signal's type: tow signals, the first one is sinusoidal with zero phase, and the second is sinusoidal with digitally controlled phase in the range $(\Delta\varphi = 0 \ldots .2\pi)$.
-Frequency Range: (3Hz…..10 MHz).
-Frequency Resolution: (3 Hz).
- Phase resolution: $(3.75 * 10^{-7}\ Rad)$
-Signal amplitude: (5 V).
-Values of phase codes (X_φ) for deference phase shift $(\Delta\varphi)$ are recorded in table (1).

Table (1): Values of phase codes (X_φ)

Num	Sel	Phase Shift (Degrees) , $(\Delta\varphi)$	Code of phase shift (X_φ)
0	000	0	0
1	001	45	2097152
2	010	90	4194304
3	011	135	6291456
4	100	180	8388608
5	101	225	10485760
6	110	270	12582912
7	111	315	14680064

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The block diagram of the DODDFS [4] is explained in figure (1), the functional diagram of the DODDFS is explained in figure (2), and the functional diagram of the DODDFS using Quartus II9.1 [5]is explained in figure (3).

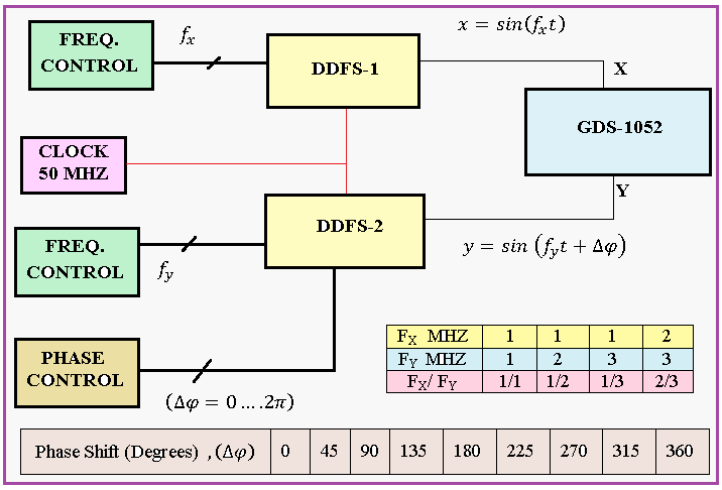

figure (1) block diagram of the DODDFS

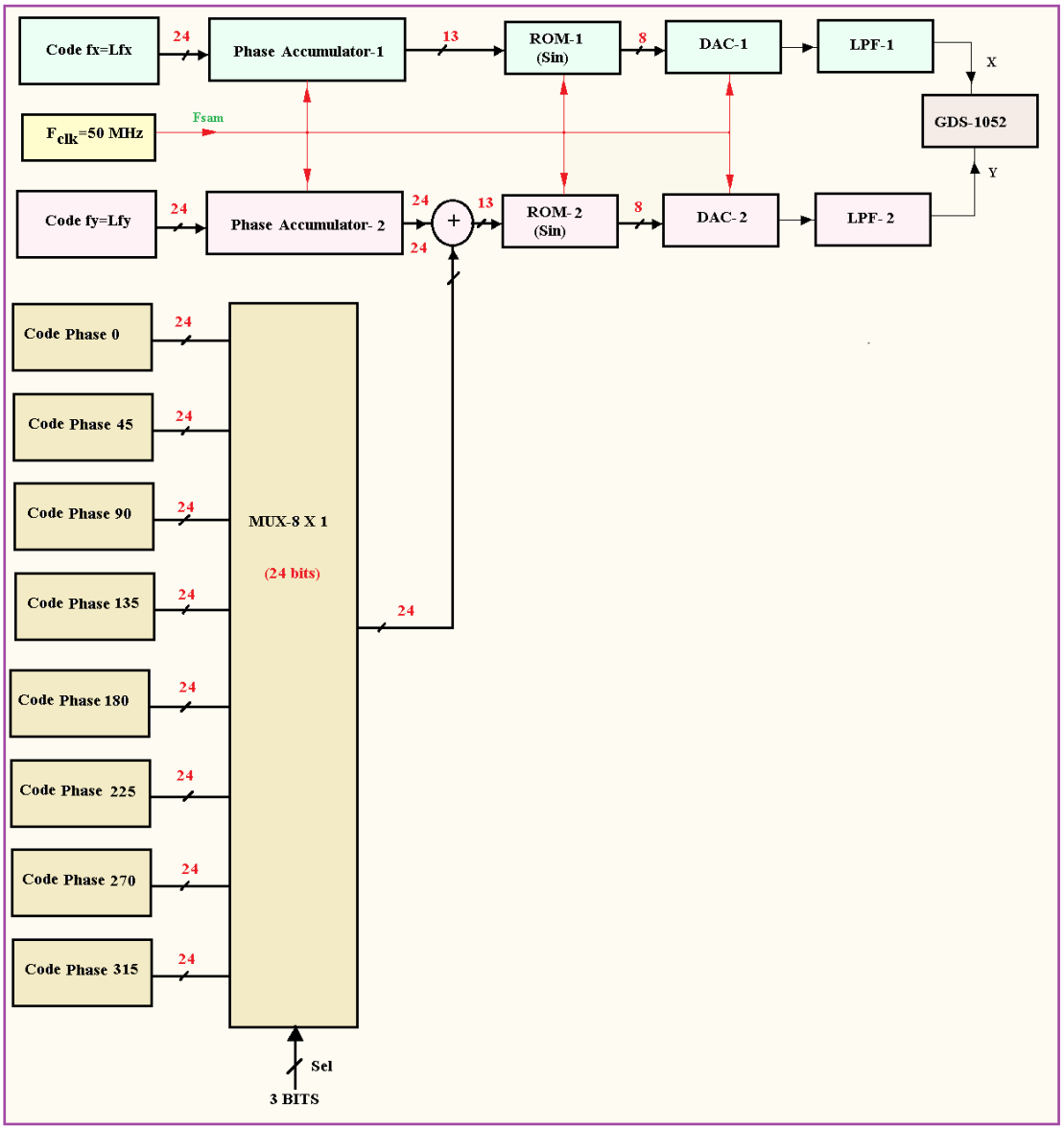

figure (2) functional diagram of the DODDFS

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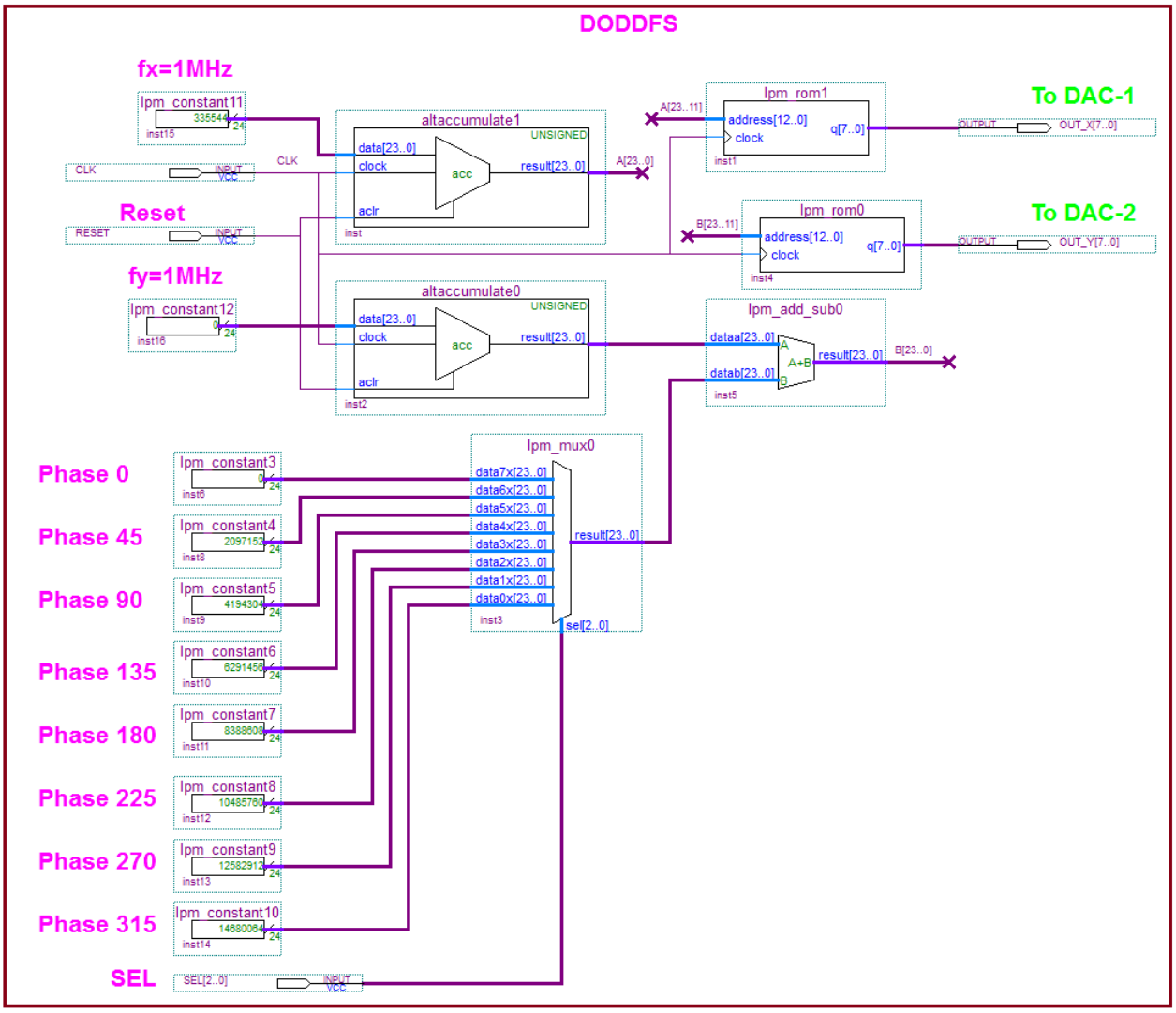

figure (3) functional diagram of the DODDFS using Quartus II9.1

The practical results of the DODDFS for f_x=1MHz , f_y =1MHz (f_x/f_y=1/1) and phase shift (0,45,90,135,180,225,270,315,360^0) are explained in figure (4) .
The practical results of the DODDFS for f_x=1 MHz , f_y =2 MHz (f_x/f_y=1/2) and phase shift (0,45,90,135,180,225,270,315,360^0) are explained in figure (5).
The practical results of the DODDFS for f_x=1MHz , f_y =3 MHz (f_x/f_y=1/3) and phase shift (0,45,90,135,180,225,270,315,360^0) are explained in figure (6).
The practical results of the DODDFS for f_x=2MHz , f_y =3 MHz (f_x/f_y=2/3) and phase shift (0,45,90,135,180,225,270,315,360^0) are explained in figure (7).

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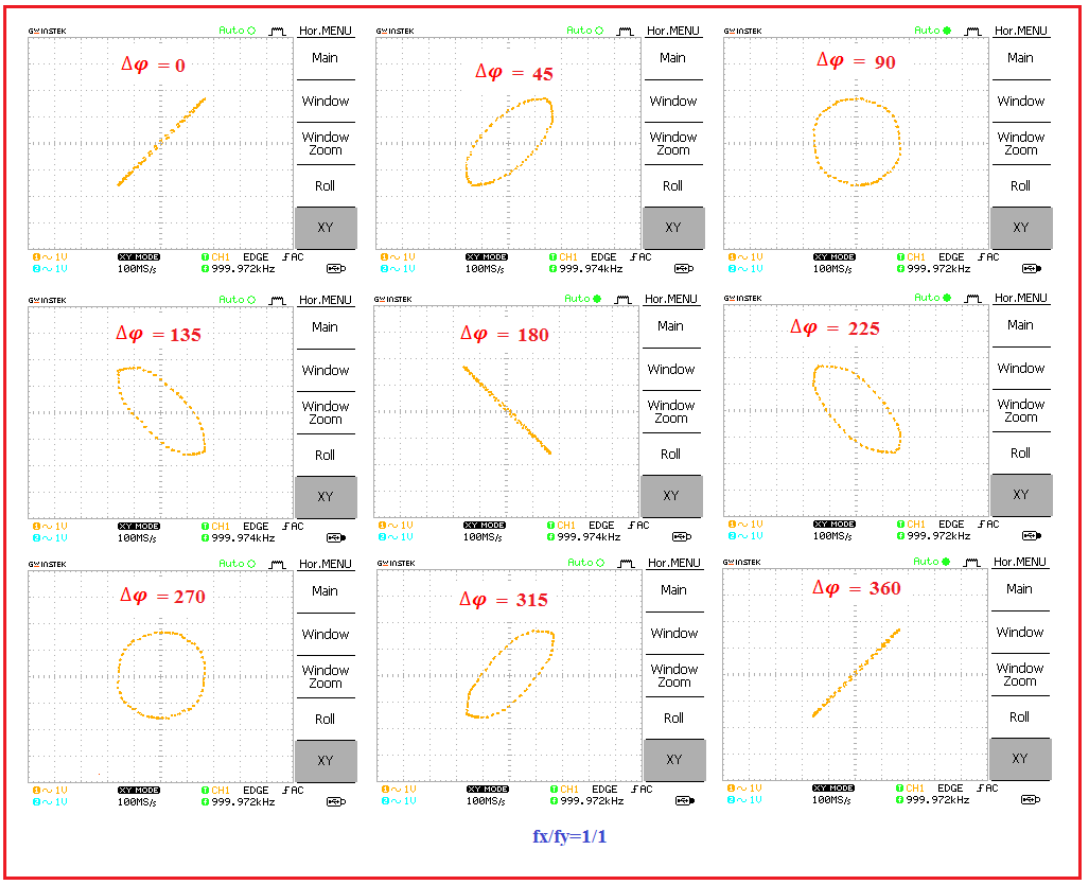

Figure (4) Lissajous figures for (f_x/f_y=1/1)

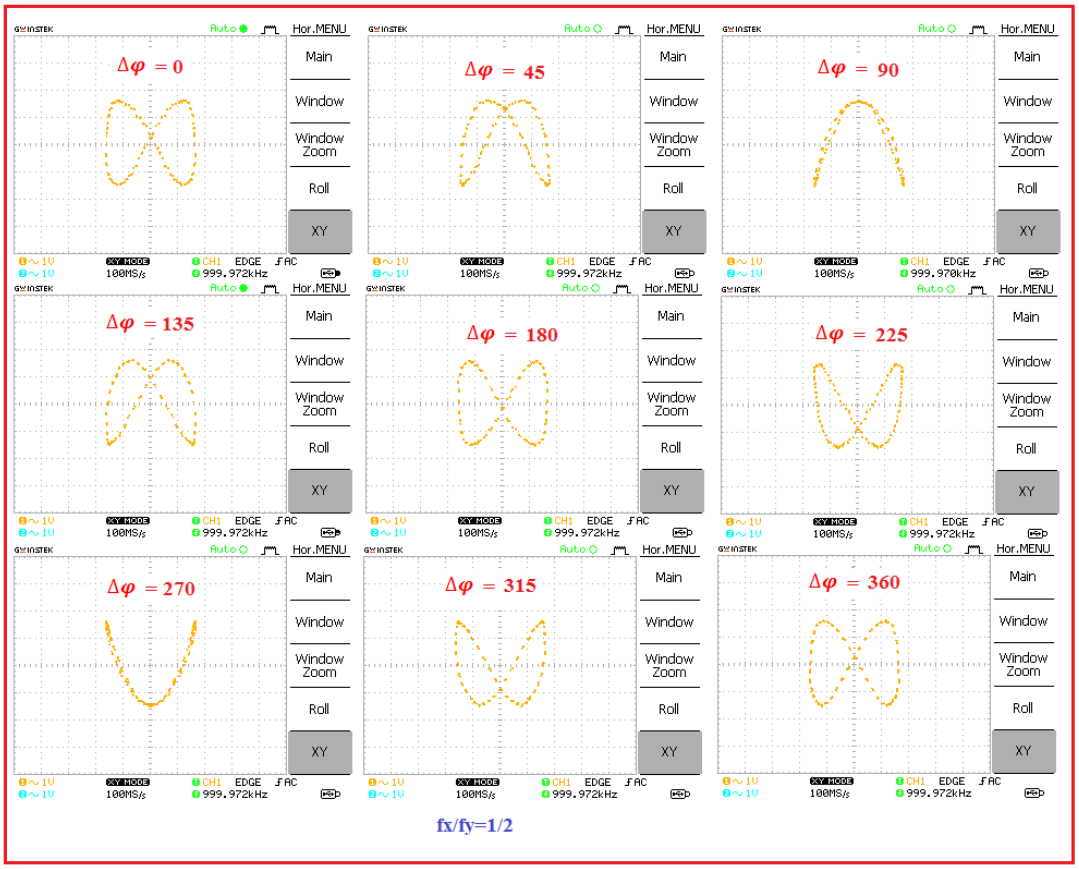

Figure (5) Lissajous figures for (f_x/f_y=1/2)

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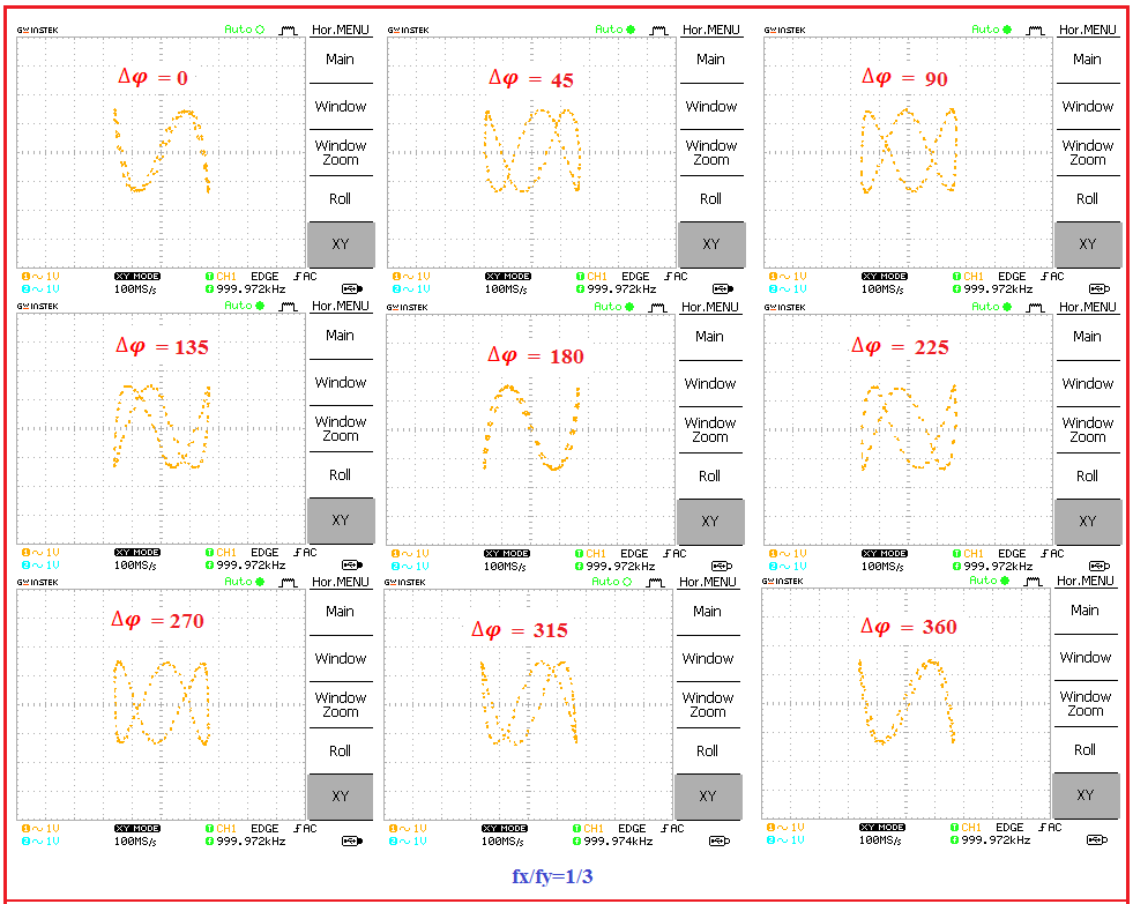

Figure (6) Lissajous figures for (f_x/f_y=1/3)

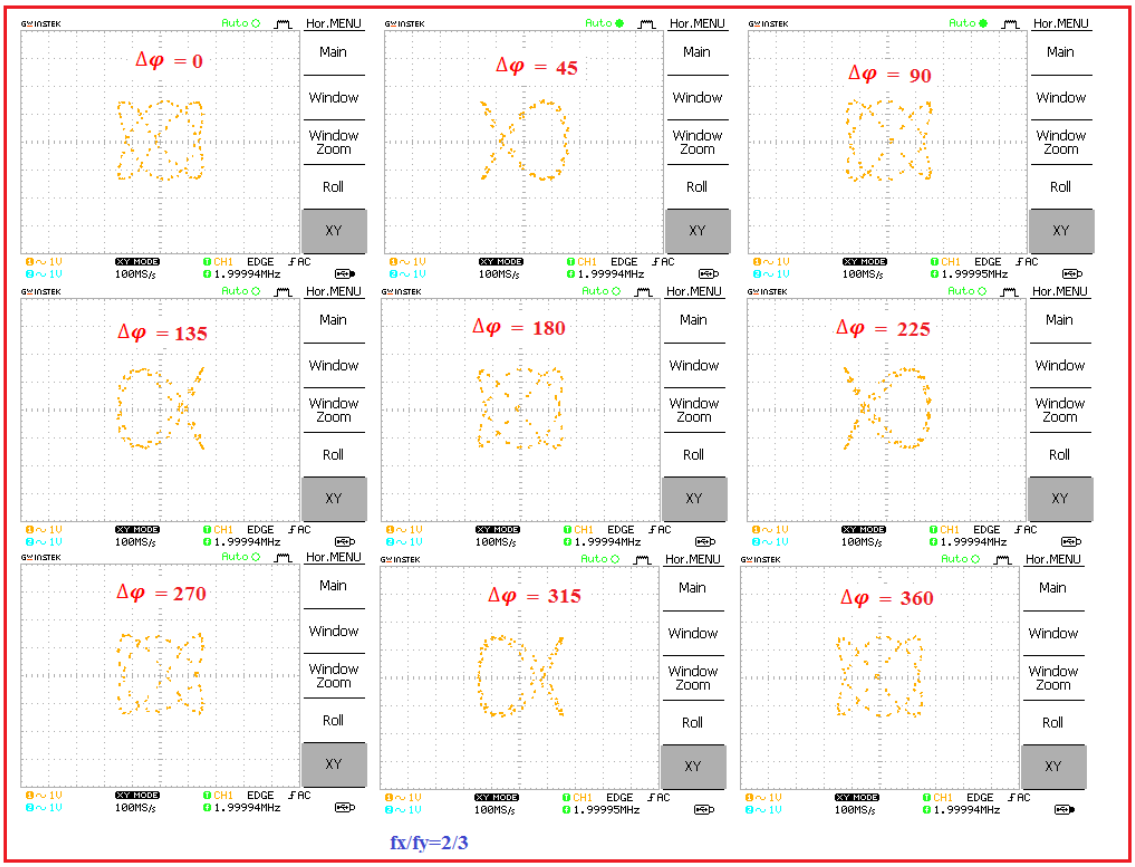

Figure (7) Lissajous figures for (f_x/f_y=2/3)

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V. CONCLUSION AND RESULTS

Based on the theoretical analysis and practical application conducted in this research, some important points can be drawn, which are summarized as follows:

-The use of DODDFS allows for the generation of any frequency ratio between the two signals, no matter how high, within the synthesizer's operating frequency range. It also enables the phase shift of the first signal to any value within the range of 0 to 360 degrees, and high-speed signal processing to obtain the desired Lissajous shapes.

-The use of FPGAs in the design process allows easy modification of the design, its specifications, and its improvement upon request, simply by changing the software design.

-Any type of signal can be modeled with very high precision, regardless of its complexity, requiring only a formula to describe the signal mathematically, tabular, graphically or otherwise.

-The frequency accuracy of DODDFS can be increased by increasing the number of bits in the synthesizer.

-The shape of the generated signal can be improved by increasing the capacity of the read-only memory (ROM) and the number of bits in the digital-to-analog converter (DAC).

-The design can be developed to obtain two signals with a variable phase shift within the range (0…360) and a phase step of less than one degree to obtain Lissajous figures.

-In this research, the laboratory experiment is designed for frequency ratio (fx/fy=1/1, 1/2, 1/3, 2/3) and phase shifts (0, 45, 90, 135, 180, 225, 270, 315,360) degrees.

-The possibility of developing the design for any frequency ratio and for any phase shift between the two signals, as well as the possibility of digitally controlling the amplitude of each of the two signals independently.

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BIOGRAPHY

Dr. Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR, university of communication in Leningrad, holds a degree assistant professor in 2009 from Aleppo university.
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