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Design and Implementation of a FIR Digital Multiband Filter (MBF) using FPGA

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Abstract: Digital signal filtering is used in many different fields, including communications, radar, navigation and others, because of its excellent performance and the ability to obtain accurate results using FIR and IIR filter

In this paper, we propose the design and implementation mechanism for FIR digital MBF based on the use of Cyclone II EP2C20F484C7 FPGA from ALTERA, placed on education and development board DE-1. The designed filter has the following parameters**:**

-Clock frequency: F_{CLK}=50 MHz.
-Sampling frequency: fsam= 2 MHz.
-Pass bands of the multiband filter (MBF): (0 -50 KHz), (100 -150 KHz), (200 -250 KHz) , (300 -350 KHz).
-Stop bands of the multiband filter (MBF): (50-100 KHz), (150 -200 KHz), (250 -300 KHz) , (350 -1000 KHz).
-Type of input signal is sinusoidal of frequency: finp=25 KHz, 75 KHz ,125 KHz, 175 KHz, 225 KHz, 275 KHz, 325 KHz
and 375 KHz.
-The ROM capacity for the stored input signal samples is 8192X8 bits, and their values are positive within the range from (0 to 255).
-Frequency range: (0.12 Hz…1 MHz).
-Frequency Resolution: (0.12 Hz).
- Signal amplitude (5V).
Digital designs using FPGA allow the system to be modified and developed to obtain better results through reprogramming according to the user's desire.

Keywords: digital filter, FIR, MBF, DDFS, FPGA.

I. INTRODUCTION

Multiband filters have been studied extensively to meet the increasing demands in areas such as satellite systems and modern communication systems where non-contiguous channels are transmitted to the same geographic area through one beam. The typical approaches to realize multi-pass band filters are:

1- The first approach is to design a number of classical single-band band pass filters, and then connect them together through input/output power splitter/combiner. However, this simple approach comes with a cost of overall circuit size and power loss due to the input-single splitting process
2- the second approach is achieved by cascading a wide band pass filter and several stop band filters, this approach has problem of interference between individual filters.
3- the third approach (utilized in our research) relies on designing a single circuit realizing the multiband characteristic. The advantage of this approach is that it uses a single component incurring a lower mass and volume and it also eliminates the need of inter-stage matching required by the other approaches.

FPGA is considered as one of the distinctive tools for designing digital filters, because it contains a large number of logical elements. It is possible to design digital filters with a high order. Multi-shape windows can also be used to improve specifications of digital filter.
In this paper, we propose a new method to replace floating-point coefficients with integer coefficients, which makes the filtering process parallel and fast, and reduces the memory capacity used to store the coefficients, and approaches the accuracy of the fractional coefficient case.
The coefficients of the designed FIR digital MBF h(n) are computed in (MATLAB) environment, and converted to signed values (-127,…,+127) with length (8) bits, then they are used in the filter design program by (VHDL) language, where

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the digital convolution algorithm of the FIR digital MBF is implemented for impulse response samples of length (N=601) as shown in figure (1), where(Z^{-1}) represents a digital delay line of length (8) bits and a delay time equal to sampling pluses period (Tsam=0.5usec). This digital MBF is designed by (VHDL) [1] with (Quartus II9.1) programming environment according to the ideal frequency response shown figure (2).

reference [2] presents the Design and Implementation of Low-Pass, High-Pass and Band-Pass Finite Impulse Response (FIR) Filters Using FPGA, where filter order is 91, and filter band 30 KHz.

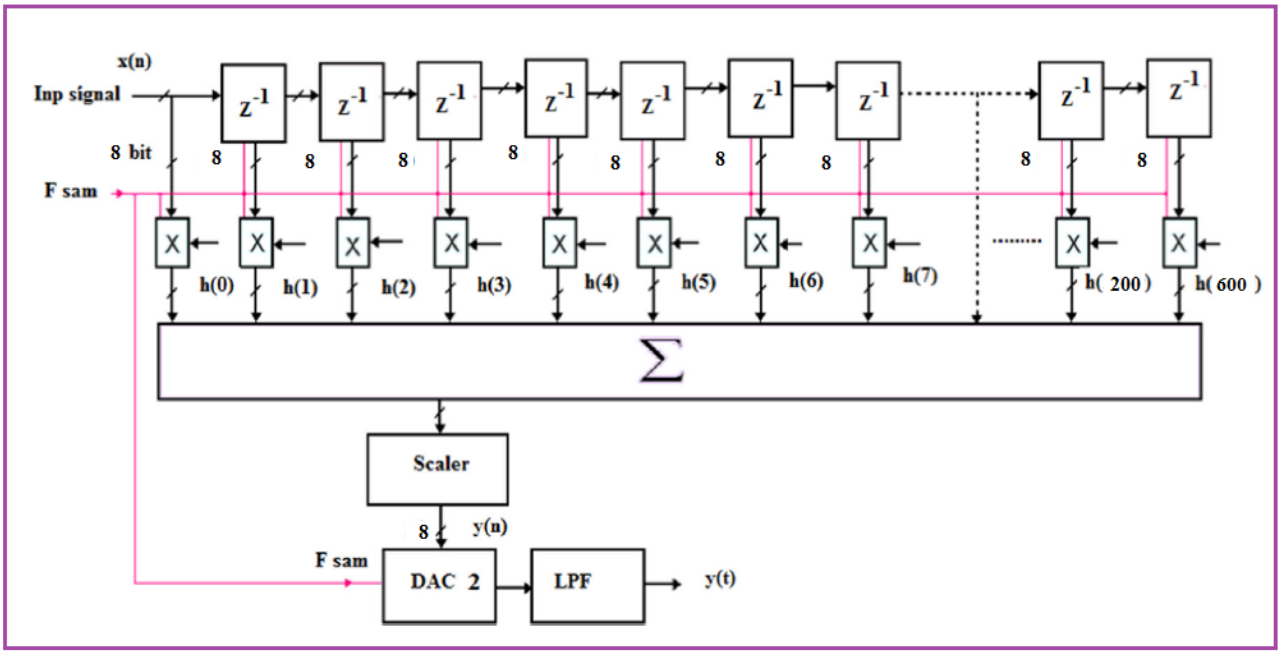

Fig. 1: The block diagram of the FIR digital filter

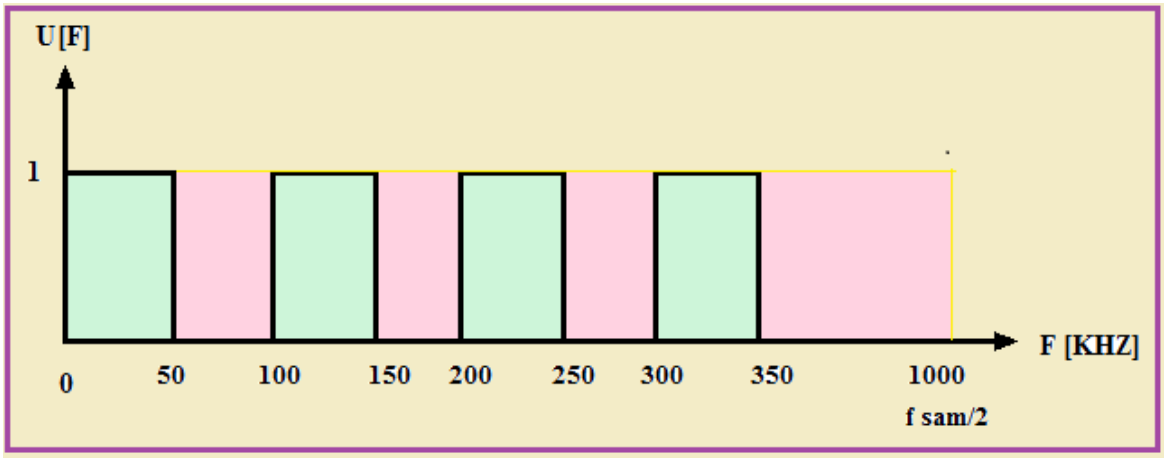

Fig. 2: The ideal frequency response of the digital MBF.

II. RESERCH IMPORTANCE AND ITS OBJECTIVES

- In this paper, FIR digital MBF was designed, implemented and tested based on the use of FPGA, VHDL and Graphical programming language of Quartus II 9.1 design environment.

- Using the digital convolution with mathematical operations (shifting, adding, multiply, division), makes the digital filters design process flexible, accurate and highly efficient.

- Changing the parameters of input signal (frequency), windows type, and filters order explains the difference between digital filters and analog filters.

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III. RESERCH MATERIALS AND ITS WAYS

The following tools and software are used to design, and test digital filters of different types (LPF, HPF, BPF, BSF, MBF), different window types, and different values of input signals:

-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].

-DDFS which is considered as a highly accuracy technique in sinusoidal and square signal synthesizing on FPGA chips.

-VHDL programming language with Quartus II 9.1 design environment.

-Design Environment MATLAB.

-GDS-1052 digital oscilloscope with Free Wave program to take the results.

-PC computer for designing and injecting the design in the FPGA chip.

The block diagram of the laboratory experiment platform [4] shown in figure (3).

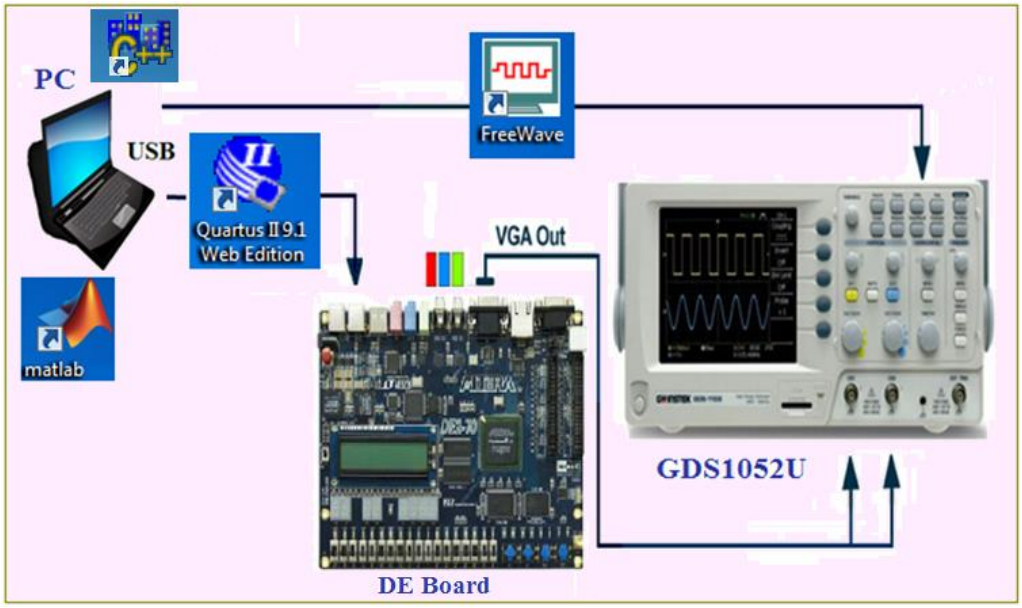

Fig (3): Block diagram of the laboratory experiment platform

IV. FILTERING ALGORITHM

The FIR digital filter output signal can be represented according to the following convolution relationship [5]:

$$y(n) = h(n) * x(n) = \sum_{k=0}^{N-1} h(k).x(n-k) \qquad (1)$$

Where: *x(n)* is the input signal samples in digital form.

N is number of samples for impulse response of the filter.
n is the sample number for input and output signals.
h(n) is the impulse response samples for digital filter.

Where:

$$n = 0, \ldots\ldots, N-1$$

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$$-\frac{(N-1)}{2} \le k \le \frac{(N-1)}{2} \qquad (2)$$

For N=601:

$$-\frac{(N-1)}{2} \le k \le \frac{(N-1)}{2} \Rightarrow -300 \le k \le 300$$

$$h_{nor}(k) = \frac{h(k)}{h_{MAX}(k)} \qquad (3)$$

$$h_{int}(k) = INT[127 * h_{nor}(k)] \qquad (4)$$

Where:

$h_{nor}(k)$ Relative value, $h_{MAX}(k) = 0.2$ Maximum value, $h_{int}(k)$ Integer value.
The values of $h(k)$ are calculated using the MATLAB environment ,Toolboxes-Filter Design-Filter Design & Analysis Tool (fdatool) , and then $h_{nor}(k)$, $h_{MAX}(k)$, $h_{int}(k)$ are recalculated according to the relationships (3) ,(4) and recorded in table (1).

Table (1)

n	0	1	2	3	4	5	6	7	8
k=n-300	-300	-299	-298	-297	-296	-295	-294	-293	-292
h(k)	-0.003069	0.001032	0.003981	0.004200	0.002348	0.000470	0.000051	0.000871	0.001602
h_{nor}(k) = h(k)/ h_{max}(k)	-0.015345	0.00516	0.019905	0.021	0.01147	0.00235	0.000255	0.004355	0.00801
h_{int}(k)= INT[127* h_{nor} (k)]	-2	1	3	3	1	0	0	1	1

.....

n	292	293	294	295	296	297	298	299	300
k=n-300	-8	-7	-6	-5	-4	-3	-2	-1	0
h(k)	0.014364	0.038686	0.035010	0.000498	-0.028674	-0.008159	0.069620	0.160356	0.20050
h_{nor}(k) = h(k)/ h_{max}(k)	0.07182	0.193425	0.17505	0.00249	-0.143365	-0.040795	0.348095	0.801775	1
h_{int}(k)= INT[127* h_{nor} (k)]	9	25	22	0	-18	-5	44	102	127

.....

n	592	593	594	595	596	597	598	599	600
k=n-300	292	293	294	295	296	297	298	299	300
h(k)	0.001602	0.000871	0.000051	0.000470	0.002348	0.004200	0.003981	0.001032	-0.003069
h_{nor}(k) = h(k)/ h_{max}(k)	0.008005	0.004355	0.000255	0.00235	0.01147	0.021	0.019905	0.00516	-0.015345
h_{int}(k)= INT[127* h_{nor} (k)]	1	1	0	0	1	3	3	1	-2

V. DESIGN OF THE DIGITAL FILTER USING MATLAB

The FIR digital multiband filter (MBF) was designed using MATLAB and VHDL with the following parameters [7]:
-Type of filter: MBF.
- Filter structure: Direct form – FIR- Least-square.
-Filter order: 600.
-Filter length: 601.

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-Sampling frequency: 2MHz.
-Frequencies of input signals: finp=25 KHz, 75 KHz , 125 KHz , 175 KHz , 225 KHz , 275 KHz , 325 KHz , 375 KHz.
-Pass bands of the multiband filter (MBF): (0 -50 KHz), (100 -150 KHz), (200 -250 KHz) , (300 -350 KHz).
-Stop bands of the multiband filter (MBF): (50 -100 KHz), (150 -200 KHz), (250 -300 KHz) , (350 -1000 KHz). .
- Type of FIR filter : Least-square.
-Word length: 8 bits.

The specification and magnitude response of a digital filter designed in MATLAB is shown in figure (4).

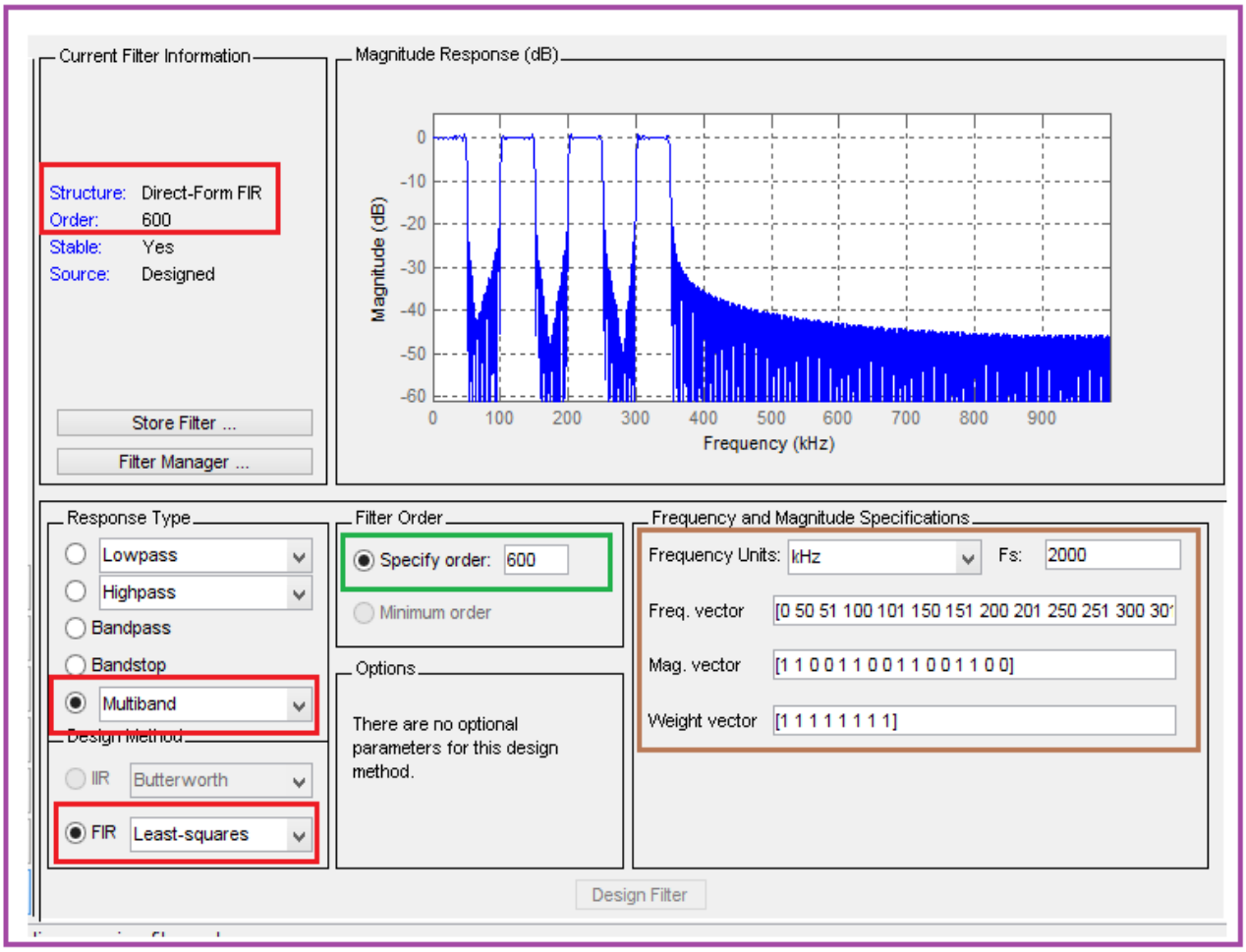

Fig (4): The specification and magnitude response of a digital multiband filter designed in MATLAB

VI. DESIGN OF THE DDFS USIGN QUARTUS II 9.1

The designed DDFS has the following parameters:

-The frequency step i : $\delta f = 0.12\ Hz$, $and\ f_{sam} = 2\ MHz$.

-The input signal is sinusoidal of frequency finp=25KHz, 75KHz , 125KHz, 175KHz, 225KHz, 275KHz, finp7=325KHz , 425 KHz, and fsam= 2 MHz.

-The ROM capacity for the stored signal samples 8192X8 bits, and their values are positive within the range from 0 to 255.

-The number of the accumulator bits is computed from the following mathematical relation [8]:

$$\delta f = \frac{f_{sam}}{2^n} \qquad (5)$$

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$$\delta f = \frac{f_{sam}}{2^n} \Longrightarrow 2^n = \frac{f_{sam}}{\delta f} = \frac{2\ X\ 10^6}{0.12} \Longrightarrow n = 24 \text{ bits}$$

-The frequency range for the DDFS is computed from the following mathematical relation:

$$\Delta f = \delta f \ldots\ldots \frac{f_{sam}}{2} = 0 \ldots 1\ MHz$$

- The frequency code is calculated according the following relation [9]:

$$Code\ f = L = \frac{f.2^{\mathrm{n}}}{f_{sam}} \qquad (6)$$

So to synthesize eight input signals of frequencies finp=25 KHz, 75 KHz , 125 KHz , 175 KHz , 225 KHz , 275 KHz , 325 KHz , 375 KH and fsam= 2 MHz, the frequency code of each one will be:

$$Code\ f_{sam} = L_{sam} = \frac{f_{sam}.2^{\mathrm{n}}}{F_{CLK}} = \frac{2\ X\ 2^{24}}{50} = 671089$$

$$Code\ f_{inp1} = L_{inp1} = \frac{f_{inp1}.2^{\mathrm{n}}}{f_{sam}} = \frac{0.025X\ 2^{24}}{2} = 209715$$

$$Code\ f_{inp2} = L_{inp2} = \frac{f_{inp2}.2^{\mathrm{n}}}{f_{sam}} = \frac{0.075\ X\ 2^{24}}{2} = 629146$$

$$Code\ f_{inp3} = L_{inp3} = \frac{f_{inp3}.2^{\mathrm{n}}}{f_{sam}} = \frac{0.125\ X\ 2^{24}}{2} = 1048576$$

$$Code\ f_{inp4} = L_{inp4} = \frac{f_{inp4}.2^{\mathrm{n}}}{f_{sam}} = \frac{0.175\ X\ 2^{24}}{2} = 1468006$$

$$Code\ f_{inp5} = L_{inp5} = \frac{f_{inp5}.2^{\mathrm{n}}}{f_{sam}} = \frac{0.225\ X\ 2^{24}}{2} = 1887437$$

$$Code\ f_{inp6} = L_{inp6} = \frac{f_{inp6}.2^{\mathrm{n}}}{f_{sam}} = \frac{0.275\ X\ 2^{24}}{2} = 2306867$$

$$Code\ f_{inp7} = L_{inp7} = \frac{f_{inp7}.2^{\mathrm{n}}}{f_{sam}} = \frac{0.325\ X\ 2^{24}}{2} = 2726298$$

$$Code\ f_{inp8} = L_{inp8} = \frac{f_{inp8}.2^{\mathrm{n}}}{f_{sam}} = \frac{0.375\ X\ 2^{24}}{2} = 3145728$$

The block diagram of the digital MBF designed in (Quartus II9.1) environment is shown in figure (5).

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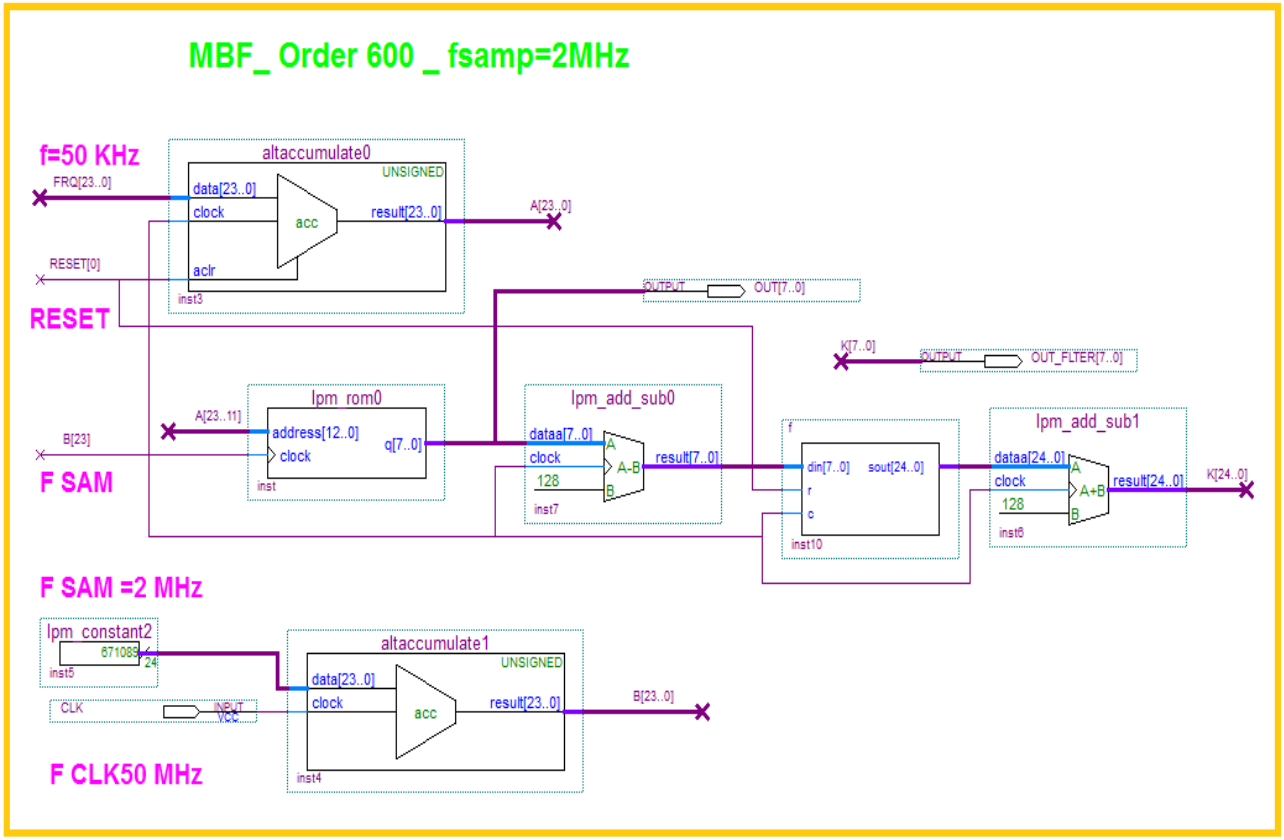

Fig (5): The block diagram of a digital MBF in (Quartus II9.1)

VII. RESULTS OF DESIG

The results of the practical design of the digital MBF for different cases (finp=25 KHz, 75 KHz , 125 KHz ,175 KHz , 225 KHz , 275 KHz , 325 KHz , 375 KHz) in time domain are shown in figure. (6). The results of the practical design of the digital MBF for the same previous cases in frequency domain are shown in figure (7), figure (8), figure (9), figure (10), figure (11), figure (12), figure (13), figure (14), figure (15), figure (16), and figure (17). These figures are taken from the screen of digital oscilloscope, and digital spectrum analyzer. We notice from these figures the identification between the theoretical results and the practical results, which indicate the high accuracy of digital synthesizing and filtering operations.

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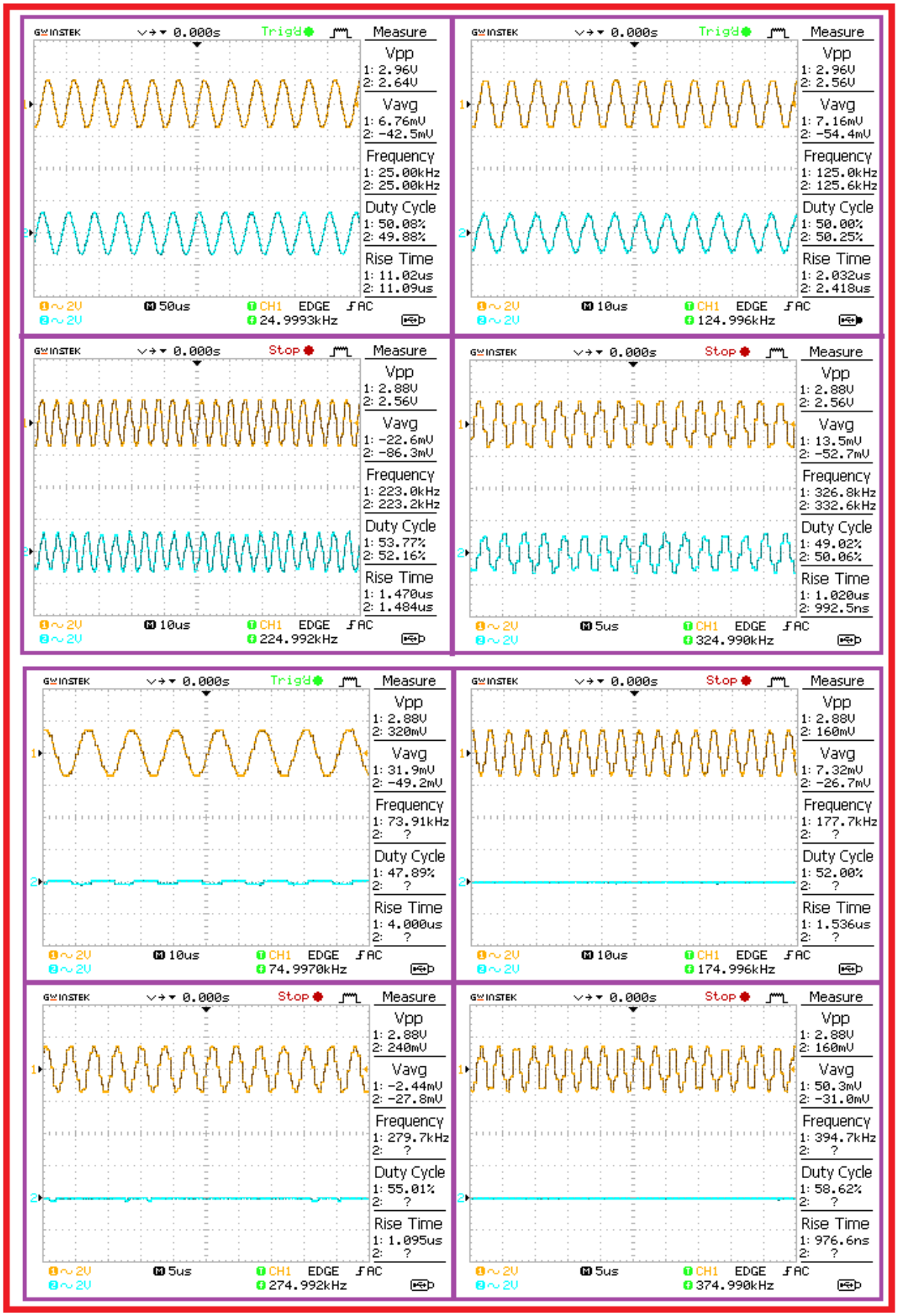

Fig. (6): The input and output signals of MBF for finp=25KHz, 75KHz, 125KHz , 175KHz, 225KHz, 275KHz, 325KHz, 375 KHz in time domain.

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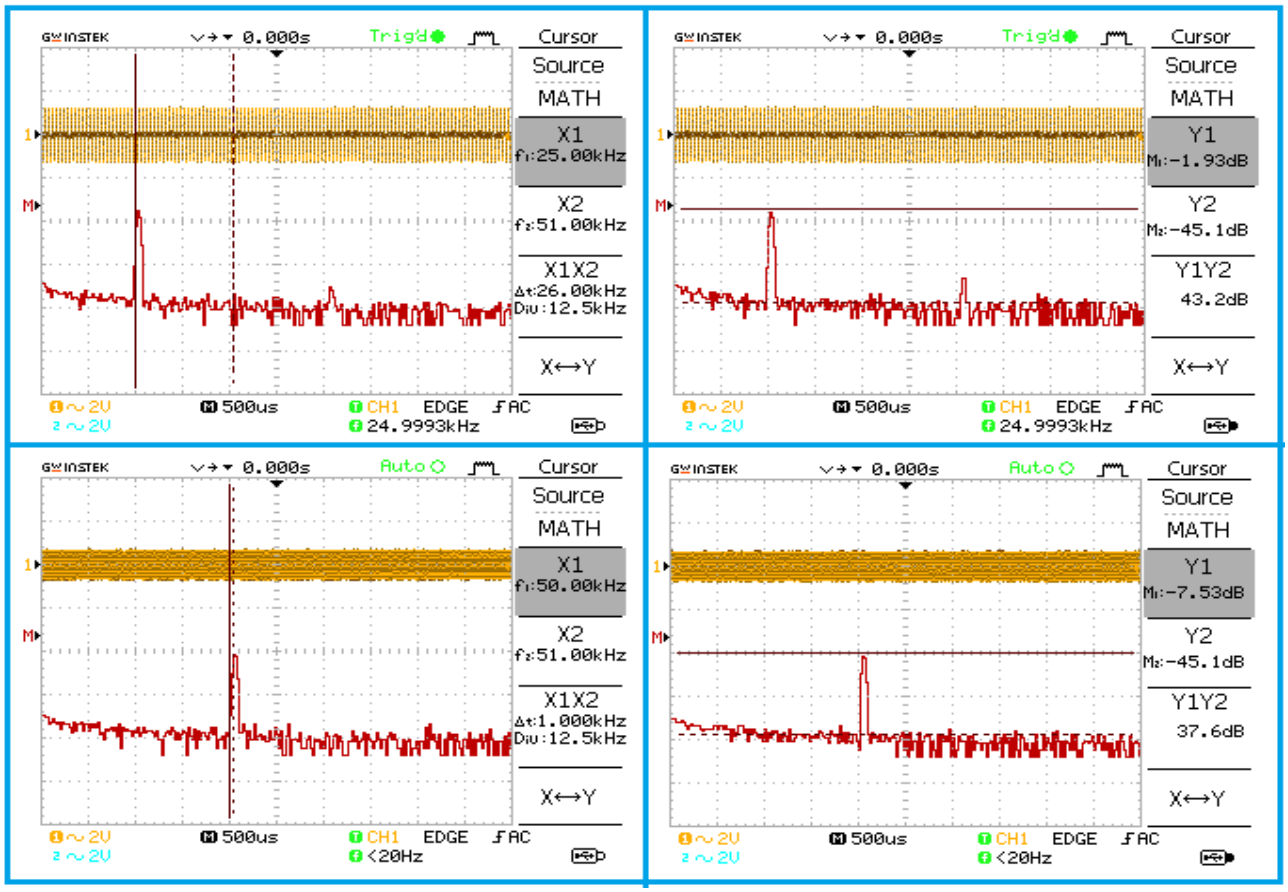

Fig. (7): The output signals for finp=25 KHz and 50 KHz in frequency domain.

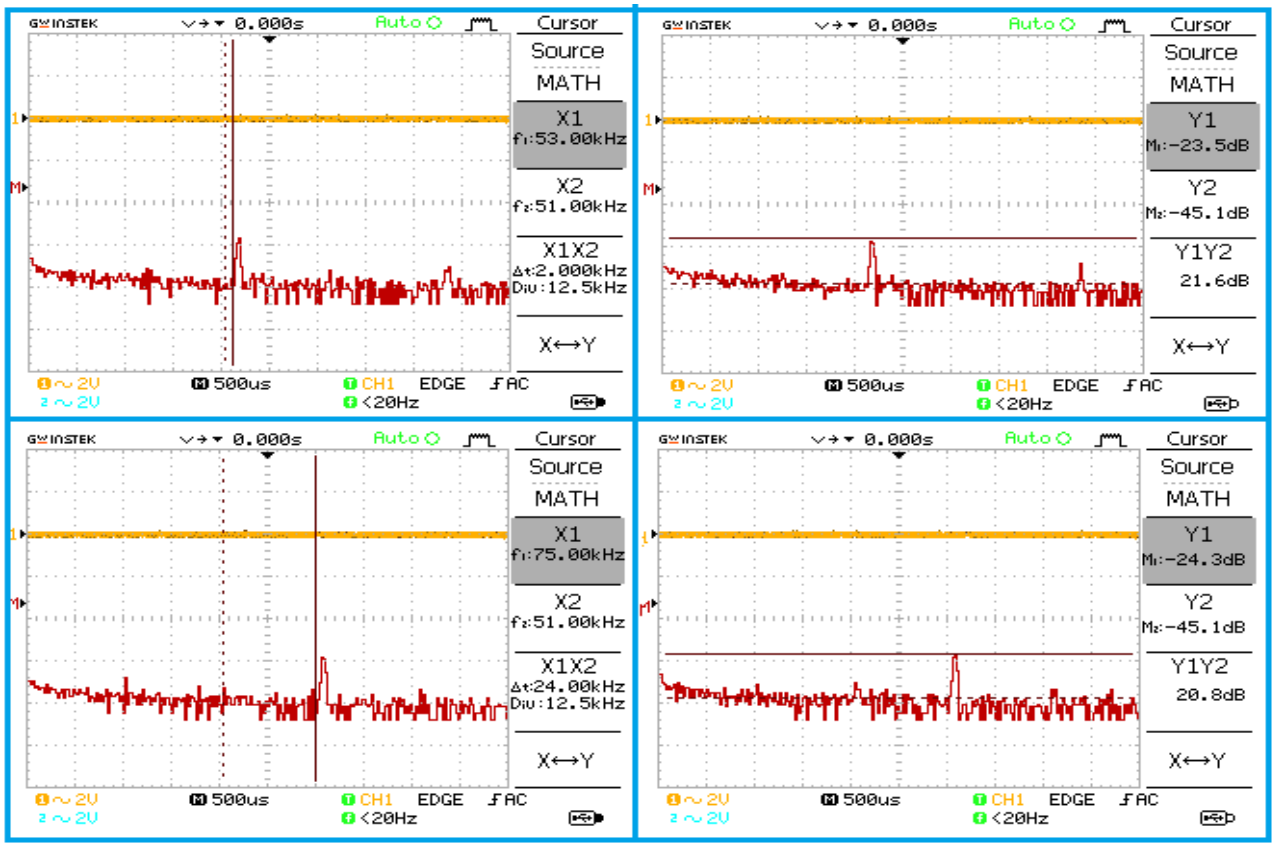

Fig. (8): The output signals for finp=53 KHz and 75 KHz in frequency domain.

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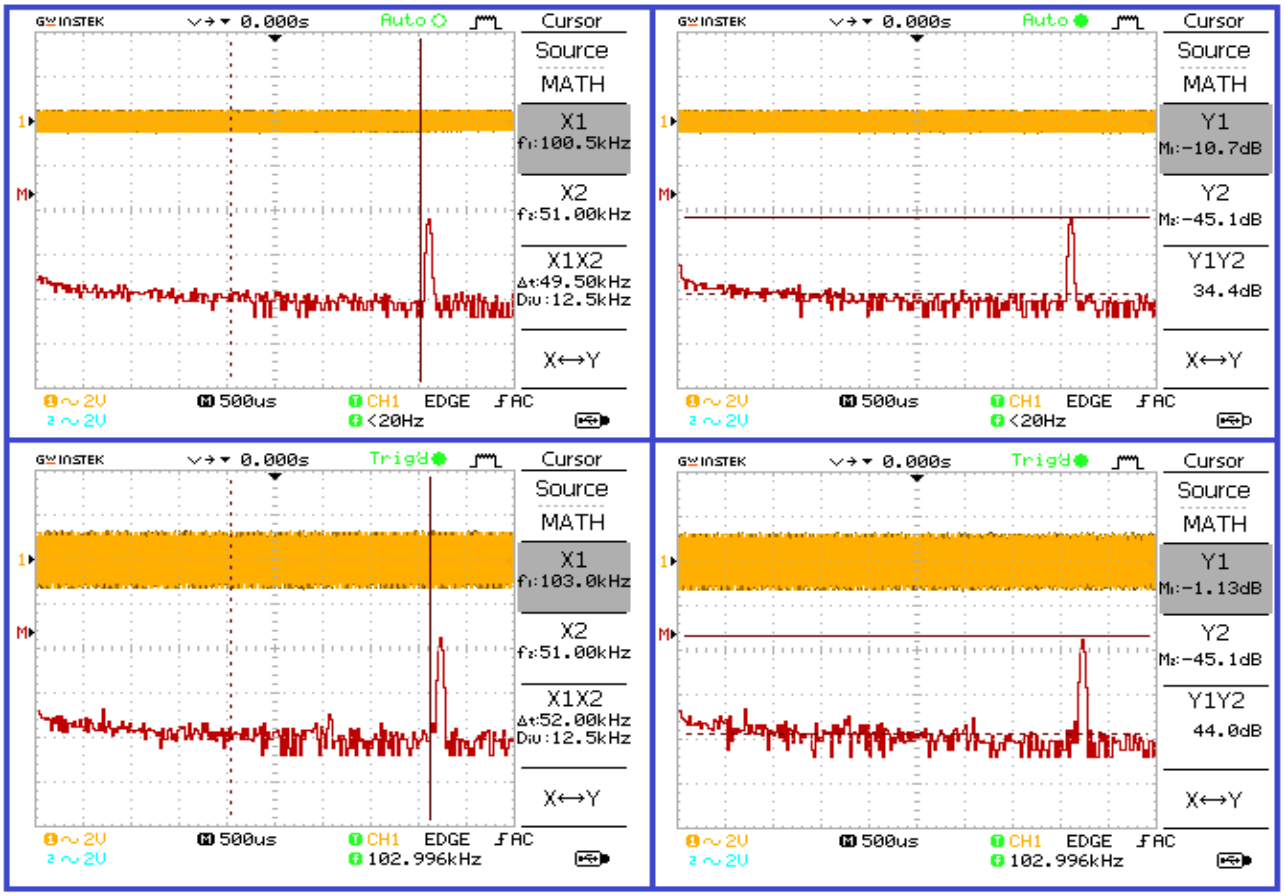

Fig. (9): The output signals for finp=100 KHz and 103 KHz in frequency domain.

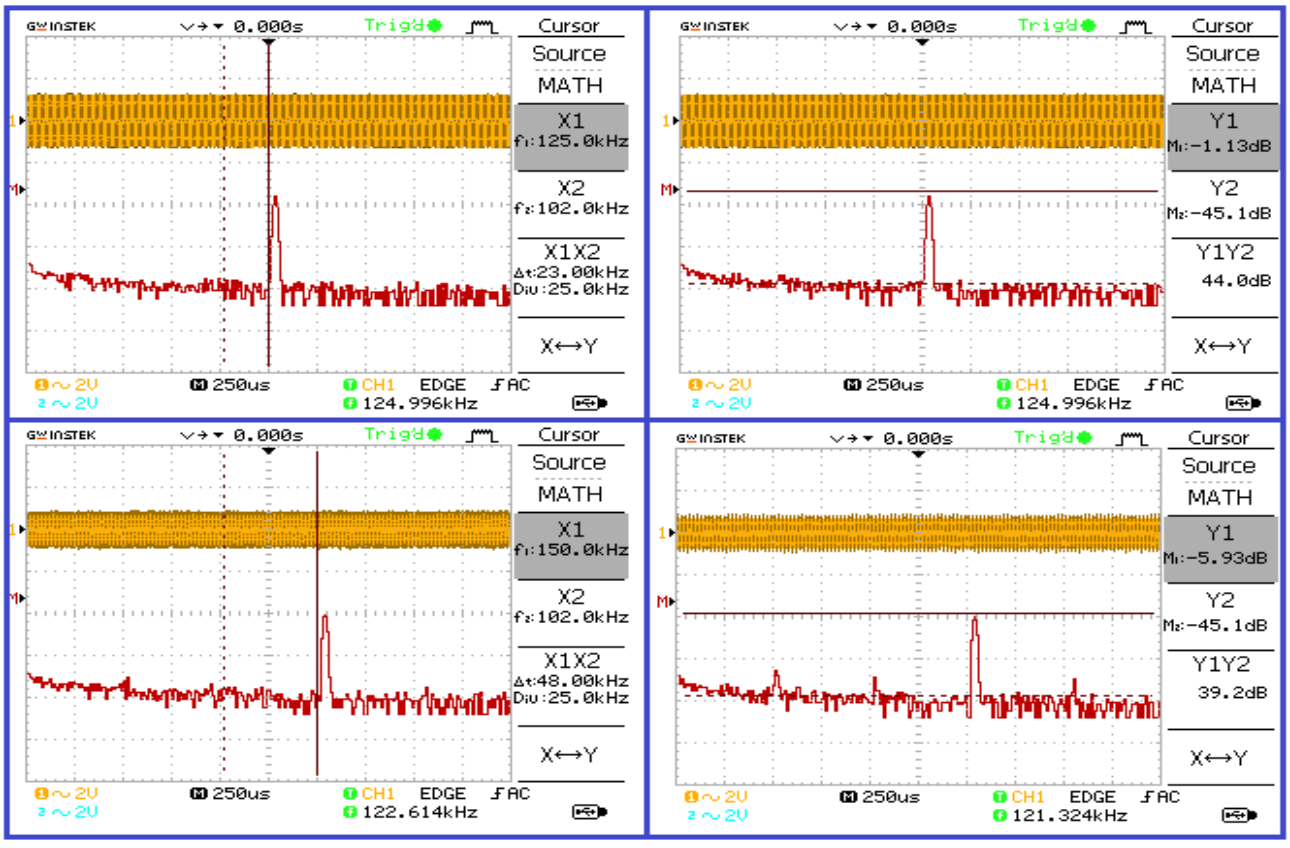

Fig. (10): The output signals for finp=125 KHz and 150 KHz in frequency domain.

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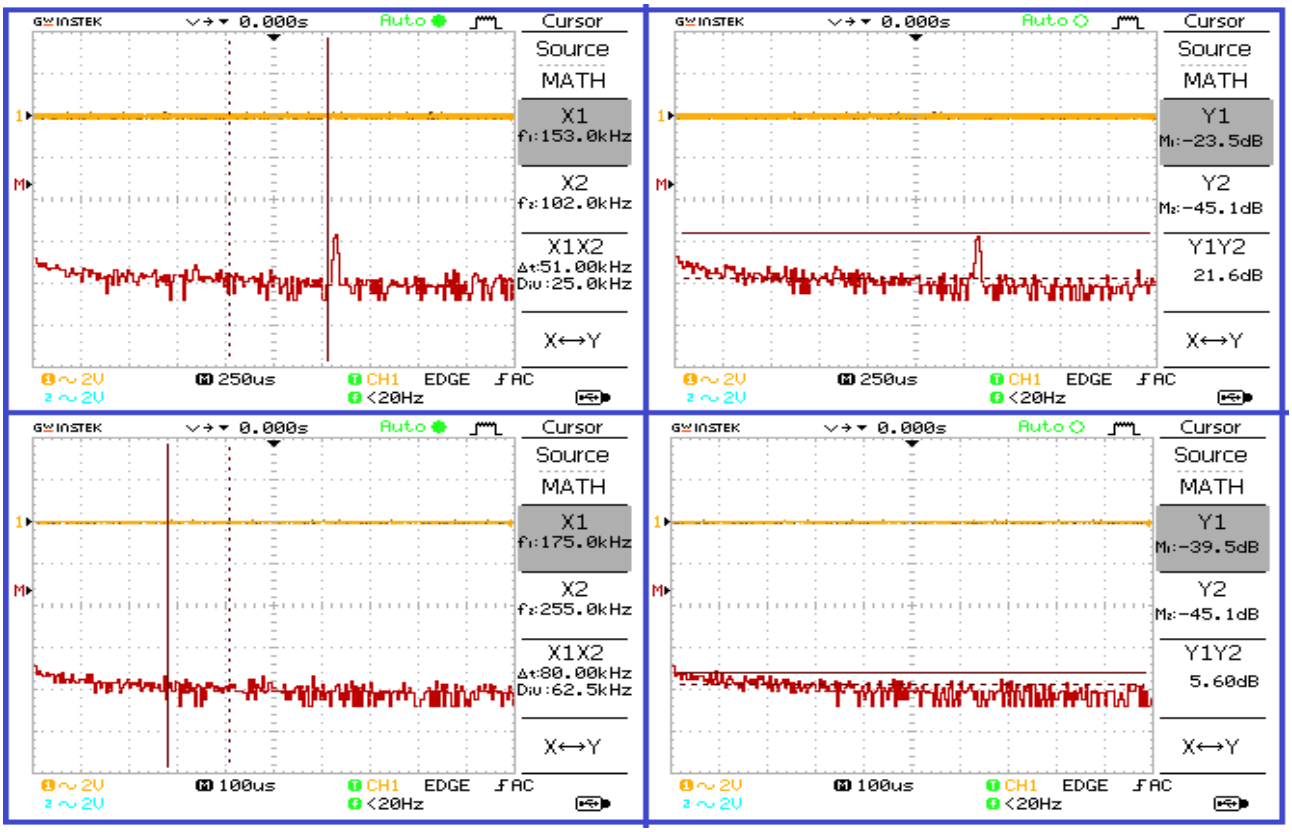

Fig. (11): The output signals for finp=153 KHz and 175 KHz in frequency domain.

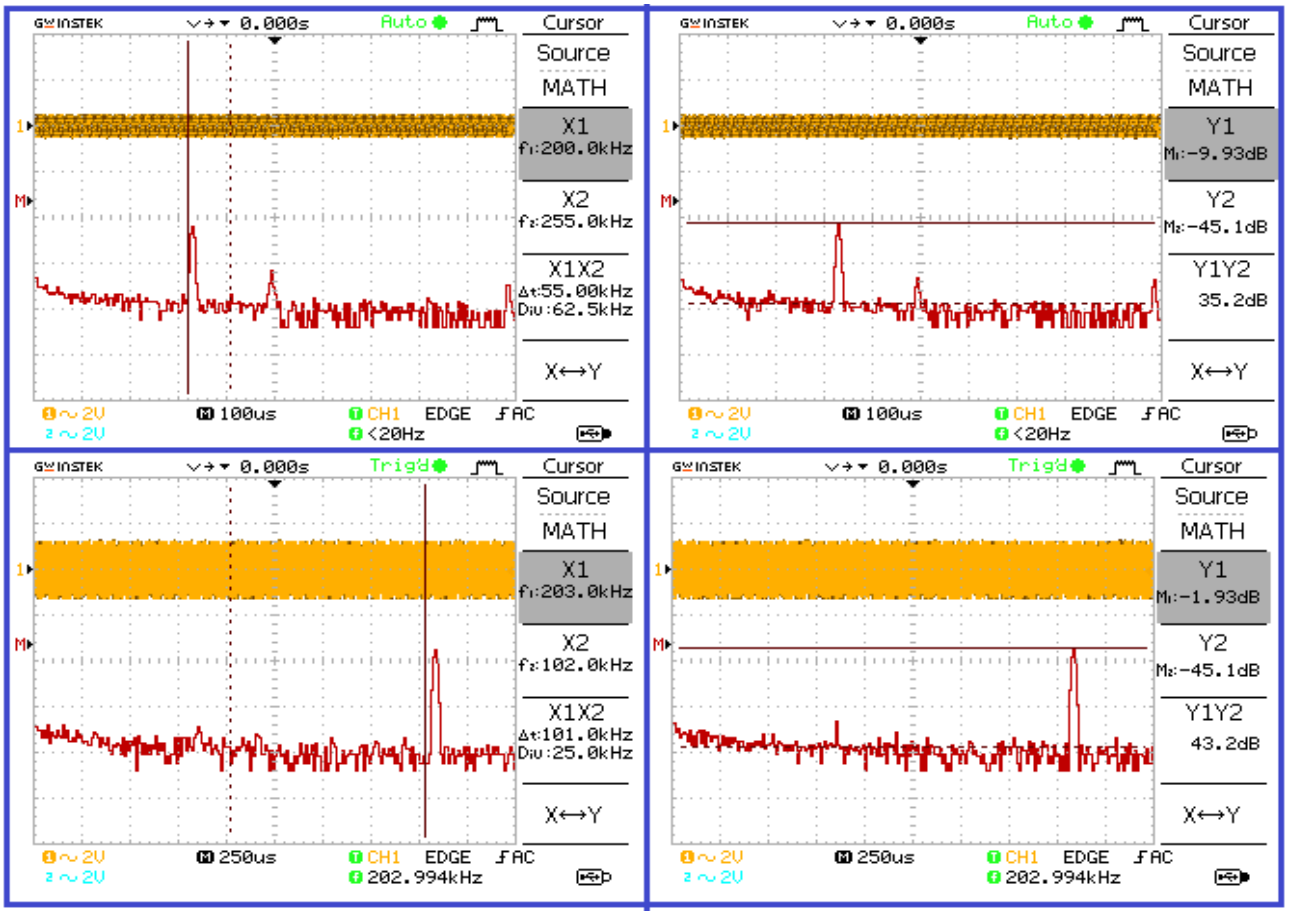

Fig. (12): The output signals for finp=200 KHz and 203 KHz in frequency domain.

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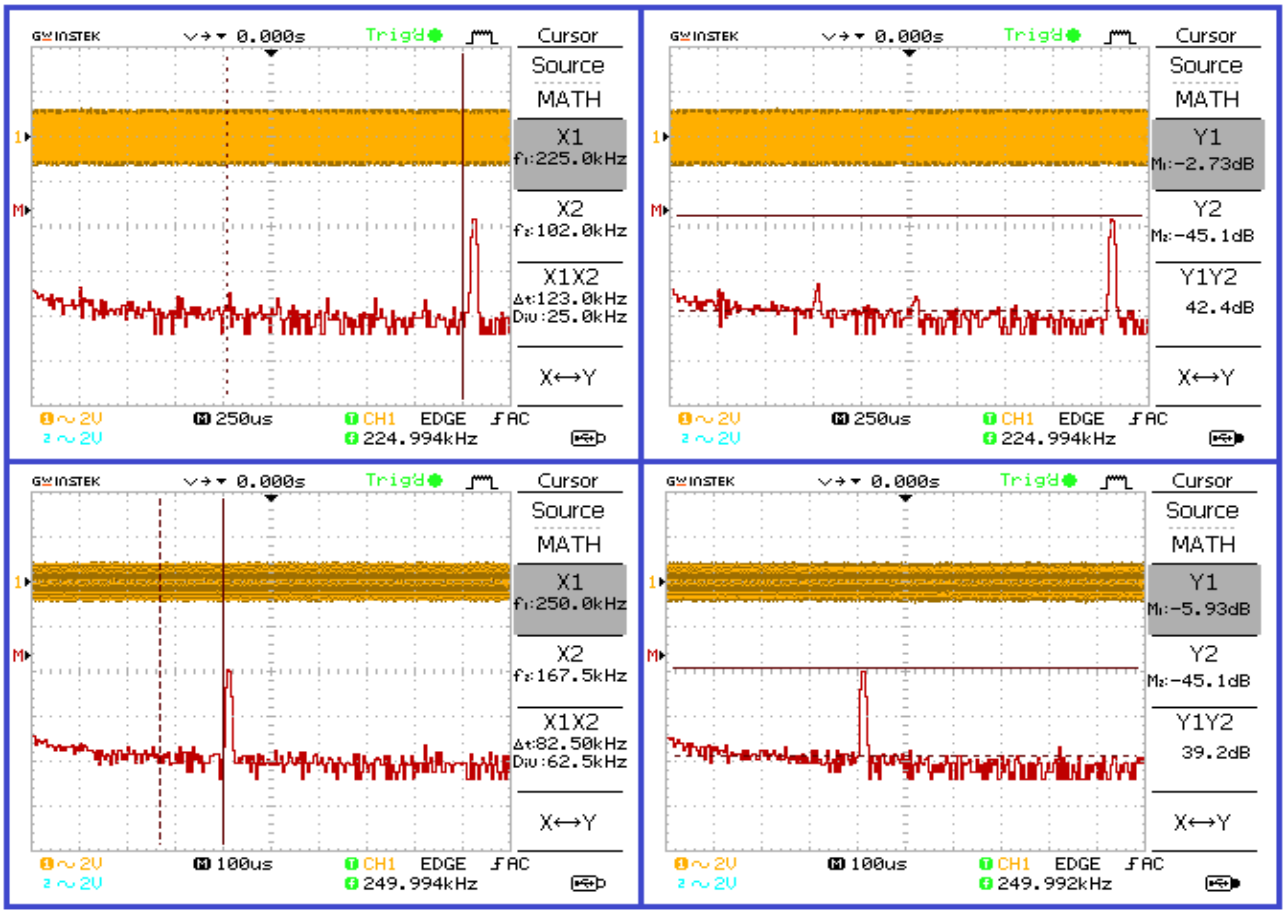

Fig. (13): The output signals for finp=225 KHz and 250 KHz in frequency domain.

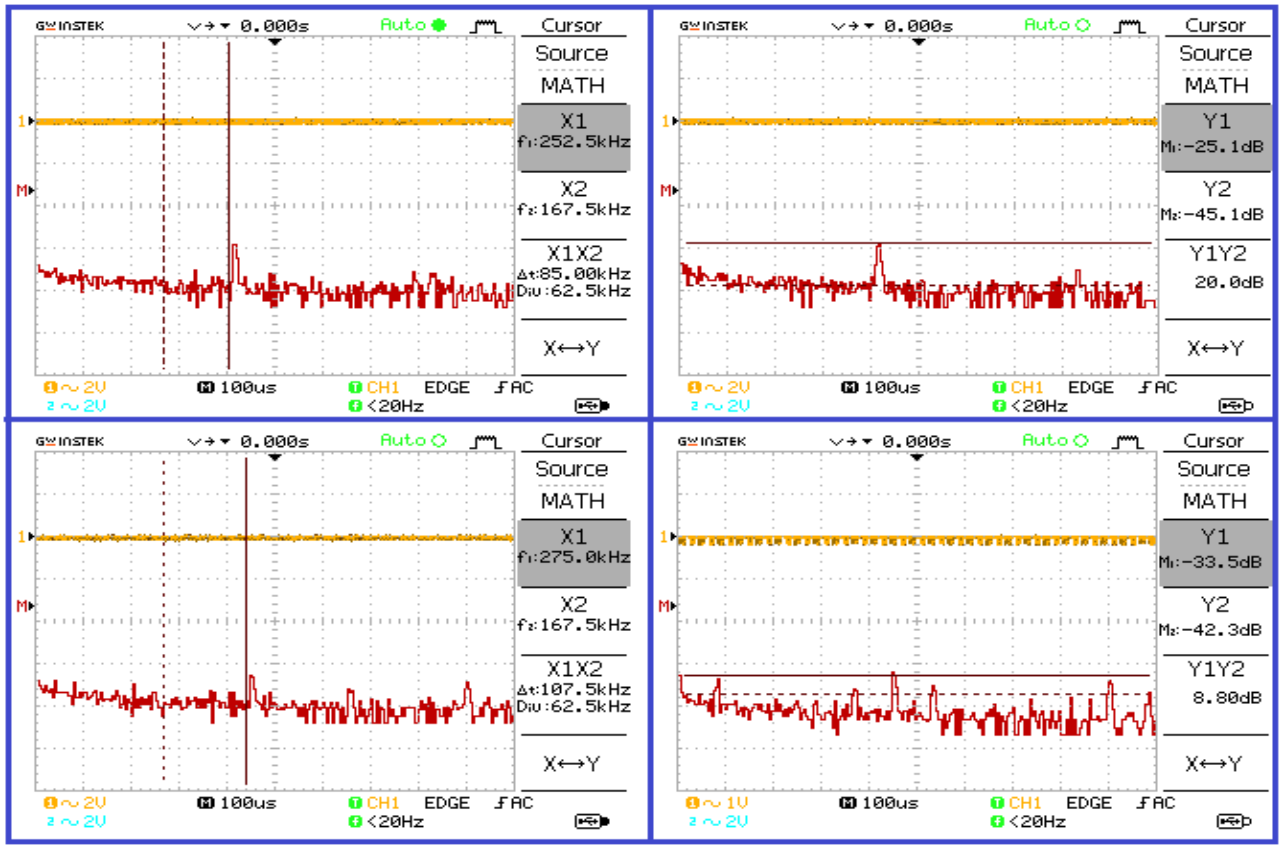

Fig. (14): The output signals for finp=253 KHz and 275 KHz in frequency domain.

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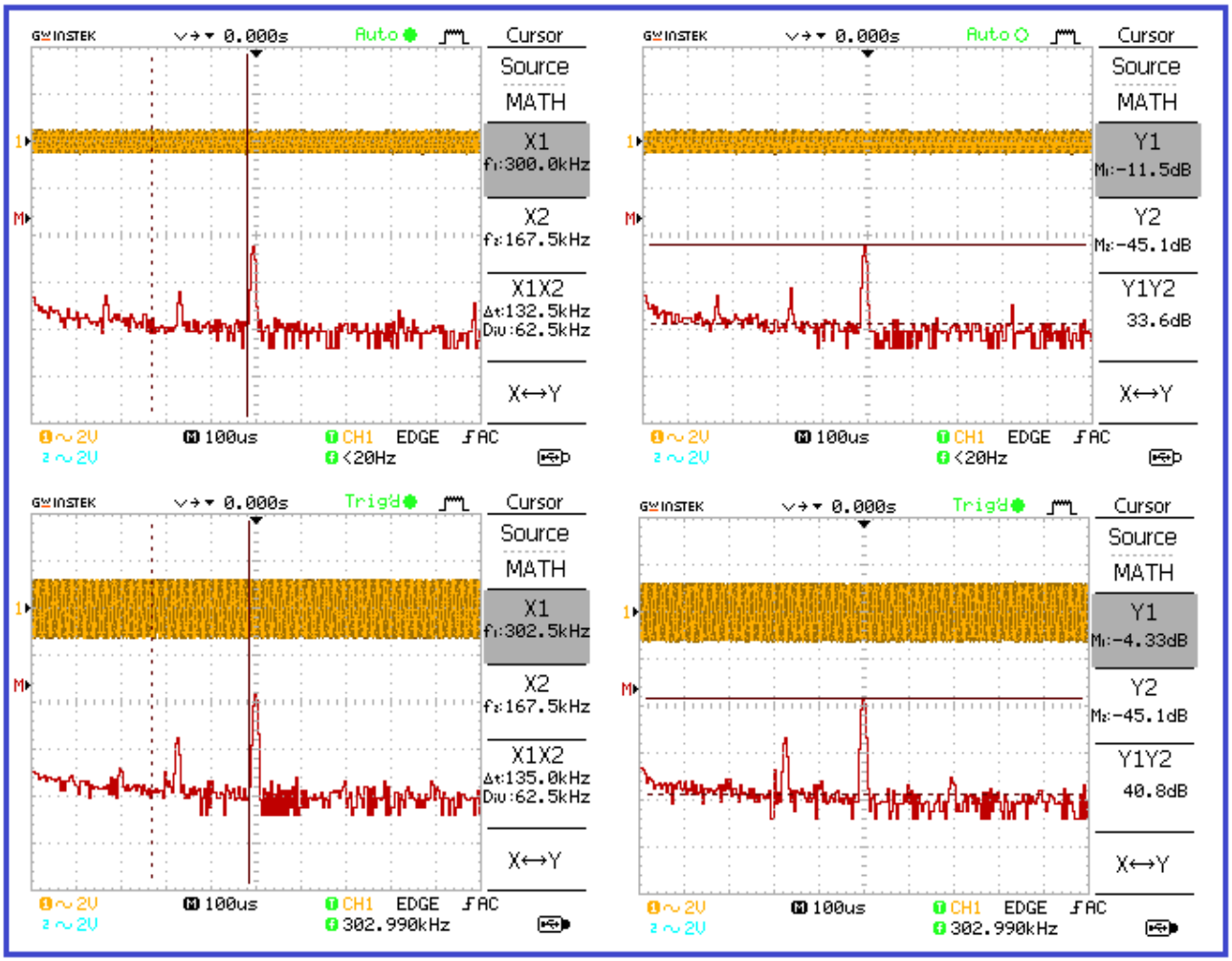

Fig. (15): The output signals for finp=300 KHz and 303 KHz in frequency domain.

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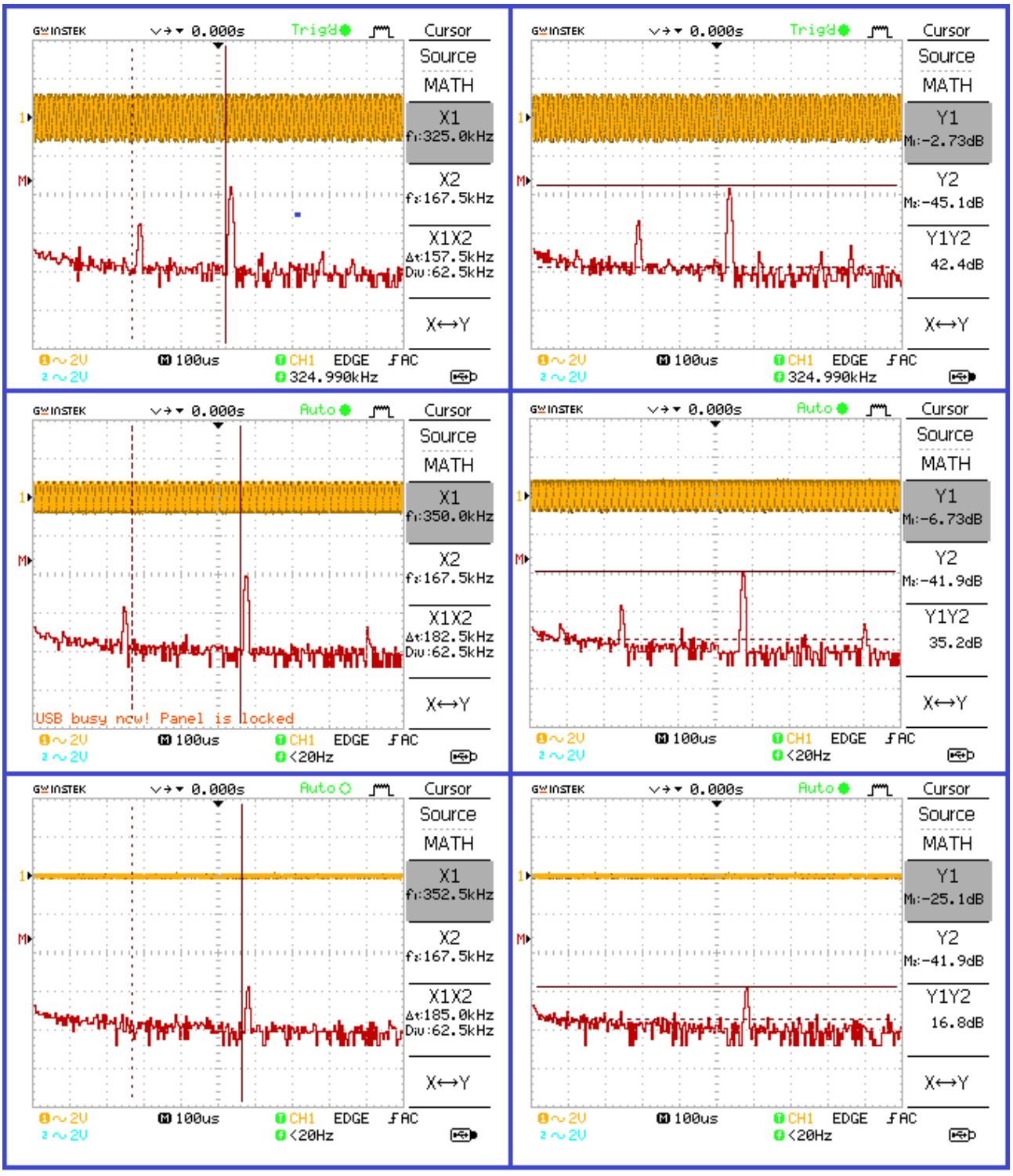

Fig. (16): The output signals for finp=325 KHz , 350 KHz and 353 KHz in frequency domain.

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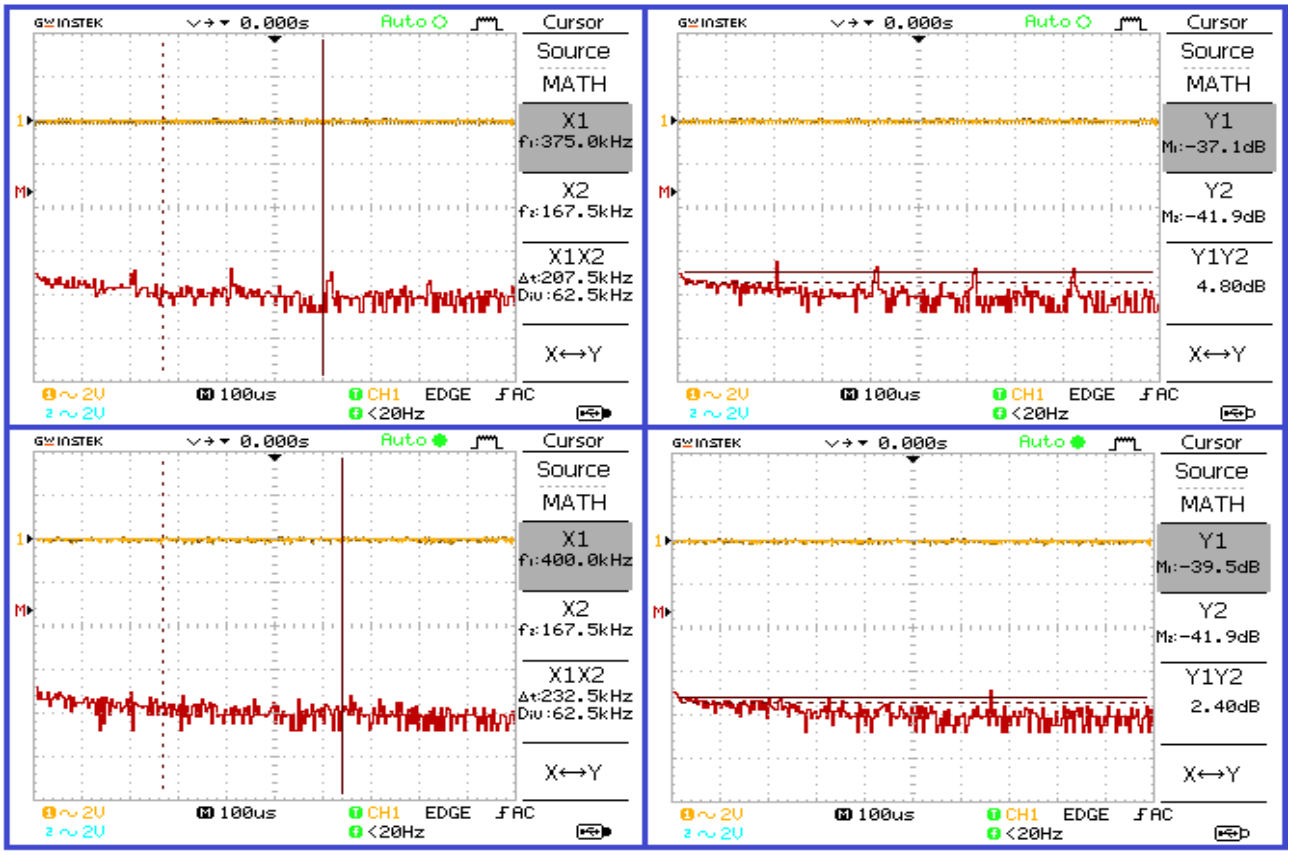

Fig. (17): The output signals for finp=375 KHz and 400 KHz in frequency domain.

The values [Uout] for different input frequencies are recorded in table (2).

Table (2)

Values [Uout] For Deference Frequency

finp [KHz]	25	50	53	75	100	103	125	150	153	175	200	203
Uout [dB]	-1.93	-7.53	-23.5	-24.3	-10.7	-1.13	-1.13	-5.93	-23.5	-39.5	-9.93	-1.93
finp [KHz]	225	250	253	275	300	303	325	350	353	375	400	450
Uout [dB]	-2.73	-5.93	-25.1	-33.5	-11.5	-4.33	-2.73	-6.73	-25.1	-39.5	-39.5	-40.0

The frequency response of the designed digital MBF is shown in figure (18).

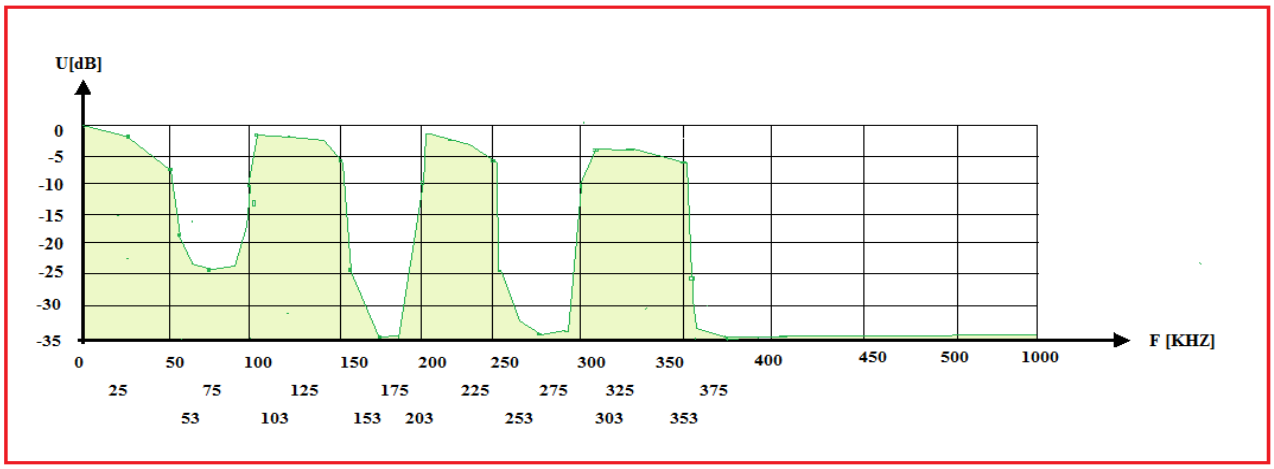

Fig. (18): The frequency response of the designed digital MBF

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From the figures we notice that the designed MBF works correctly (passes the signal of frequencies (0-50 KHz) , (100-150 KHz), (200-250 KHz), (300-350 KHz) and suppresses the signal of frequencies (50-100 KHz) **,** (150-200 KHz) , (250-300 KHz) **,** (350-1000 KHz)

VIII. DISCUSSION AND CONCLUSIONS

-Using digital filtering techniques in communication domain allows implementing different filters (LPF, HPF, BPF, BSF , MBF etc) with high accuracy and speed, and with the ability of changing parameters of signals in wide range.

-Using DDFS techniques in communication domain allows implementing the digital processing in the communication receiver on high intermediate frequency.

-We notice from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital filtering for signals.

-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).

-The most important thing in this paper is the possibility of changing the frequency of the input signals.

-The performance or specifications of a digital filter can be improved by:

- Increasing the filter order.
- Increasing the number of bits of the input signal.
- Changing the window type.

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