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Design and Implementation of a FIR Digital Moving Average Filter (MAF) using FPGA

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Abstract: Digital signal filtering is used in many different fields, including communications, radar, navigation and others, because of its excellent performance and the ability to obtain accurate results using FIR and IIR filters.

In this paper, we propose the design and implementation mechanism for FIR digital Moving Average Filter (MAF) based on the use of Cyclone II EP2C20F484C7 FPGA from ALTERA, placed on education and development board DE-1. The designed filter has the following parameters**:**

-Clock frequency: F_{CLK}=50 MHz.
-Sampling frequency: fsam= 50 MHz.
-Order filter: (32 , 128 , 512).
-$(SNR)_{inp}$ =(1/1 , 1/2 , 1/3 , 1/4) .
-Type of input signal is sinusoidal, pulse signals of frequency: finp=1 KHz .
-The ROM capacity for the stored input signal samples is (8192X8) bits, and their values are positive within the range from (0 to 255).
-Frequency range: (3 Hz…1 MHz).
-Frequency Resolution: (3 Hz).
- Signal amplitude (5V).
Digital designs using FPGA allow the system to be modified and developed to obtain better results through reprogramming according to the user's desire.

Keywords: digital filter , FIR, MAF, DDFS , DPNG , FPGA.

I. INTRODUCTION

FPGA is considered as one of the distinctive tools for designing digital filters, because it contains a large number of logical elements. It is possible to design digital filters with a high order. Multi-shape windows can also be used to improve specifications of digital filter.

In this paper, we propose a new method to replace floating-point coefficients with integer coefficients, which makes the filtering process parallel and fast, and reduces the memory capacity used to store the coefficients, and approaches the accuracy of the fractional coefficient case.

The digital summation algorithm of the FIR digital MAF is implemented for impulse response samples of length (N=512) as shown in figure (1), where (Z^{-1}) represents a digital delay line of length (8) bits and a delay time equal to sampling pluses period (Tsam=0.02usec). This digital MAF is designed by (VHDL) [1] with (Quartus II9.1) programming environment according to the ideal frequency response shown figure (2).

reference [2] presents the Design and Implementation of digital filters Using FPGA, where filter order of moving average filter is (7) only.

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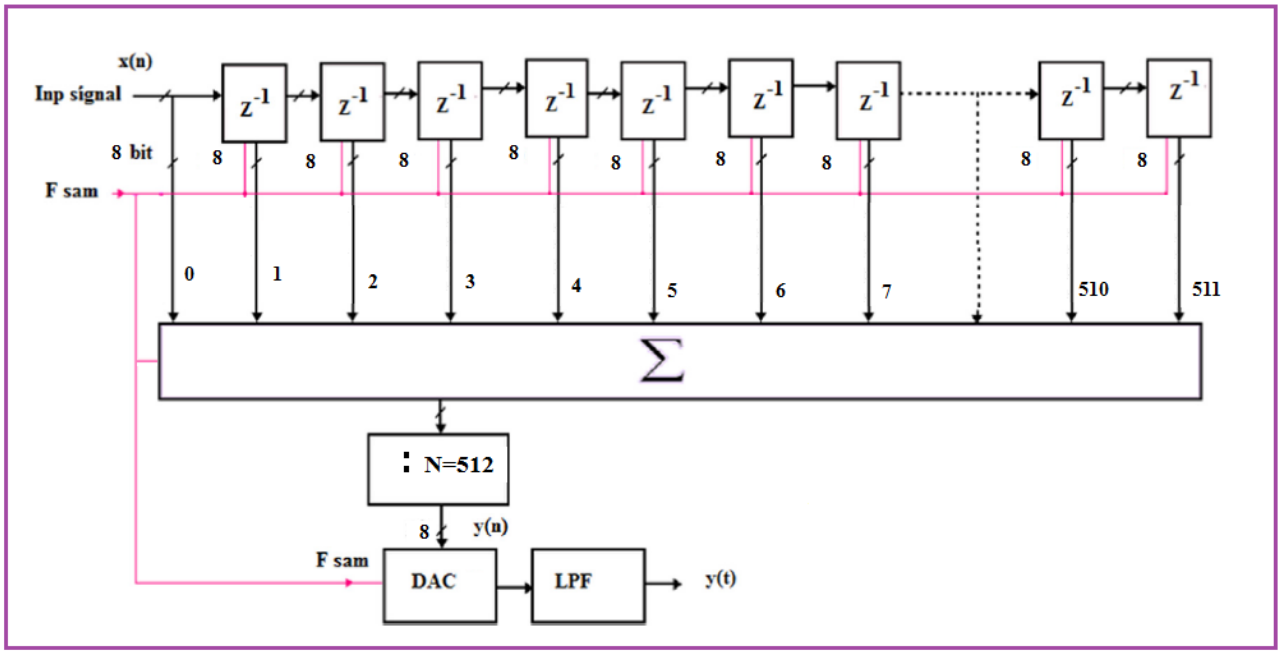

Fig. (1): The block diagram of the FIR digital moving average filter

II. RESERCH IMPORTANCE AND ITS OBJECTIVES

- In this paper, FIR digital MAF was designed, implemented and tested based on the use of FPGA, VHDL and Graphical programming language of Quartus II 9.1 design environment.

- Using the digital convolution with mathematical operations (shifting, adding, multiply, division), makes the digital filters design process flexible, accurate and highly efficient.

- Changing the parameters of input signal (frequency), and filters order explains the difference between digital filters and analog filters.

III. RESERCH MATERIALS AND ITS WAYS

The following tools and software are used to design, and test digital filters of different types (LPF, HPF, BPF, BSF, MBF ,MAF), different window types, and different values of input signals:

-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].

-DDFS which is considered as a highly accuracy technique in sinusoidal and square signals synthesizing on FPGA chips.

-VHDL programming language with Quartus II 9.1 design environment.

-Design Environment MATLAB.

-GDS-1052 digital oscilloscope with Free Wave program to take the results.

-PC computer for designing and injecting the design in the FPGA chip.

The block diagram of the laboratory experiment platform [3] shown in figure (2).

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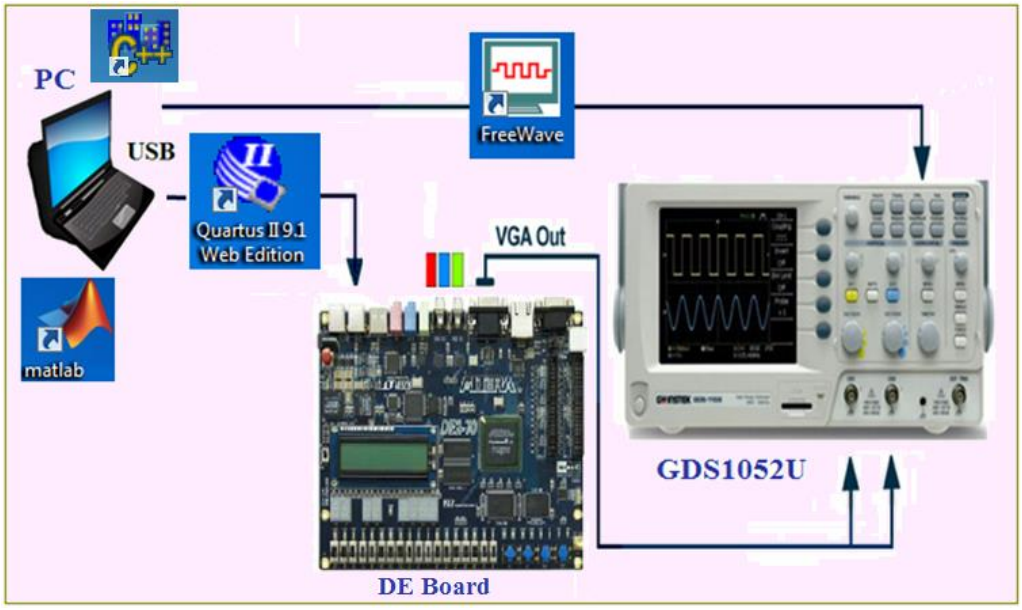

Fig (2): Block diagram of the laboratory experiment platform

IV. FILTERING ALGORITHM

The FIR digital moving average filter (MAF) output signal can be represented according to the following convolution relationship [4]:

$$y(n) = \frac{1}{N}\sum_{k=0}^{N-1} x(n+k) \qquad (1)$$

Where:

x(n) : is the input signal samples in digital form.
N : is the number of points in the average.
n : is the sample number for input and output signals.

V. DESIGN OF THE DDFS USIGN QUARTUS II 9.1

The designed DDFS has the following parameters:
-The frequency step i : $\delta f = 3\ Hz\ , and\ f_{sam} = 50\ MHz$.
-The input signal is sinusoidal of frequency finp1=1 KHz and fsam= 50 MHz.
-The ROM capacity for the stored signal samples 8192X8 bits, and their values are positive within the range from 0 to 255.
-The number of the accumulator bits is computed from the following mathematical relation [5]:

$$\delta f = \frac{f_{sam}}{2^n} \qquad (2)$$

$$\delta f = \frac{f_{sam}}{2^n} \Rightarrow 2^n = \frac{f_{sam}}{\delta f} = \frac{50X\ 10^6}{3} \Rightarrow n = 24 \text{ bits}$$

-The frequency range for the DDFS is computed from the following mathematical relation:

$$\Delta f = 0 \ldots . \frac{f_{sam}}{2} = 0 \ldots .25\ MHz$$

- The frequency code is calculated according the following relation [5]:

$$Code\ f = L = \frac{f.2^{\mathrm{n}}}{f_{sam}} \qquad (3)$$

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So to synthesize an input signal of frequency $f_{inp} = 1$ KHz and fsam= 50 MHz , the frequency code will be [6]:

$$Code\ f_{inp} = L_{inp} = \frac{f_{inp}.2^{n}}{f_{sam}} = \frac{1X\ 2^{24}}{50000} = 355$$

The block diagram of the DDFS designed in (Quartus II9.1) environment is shown in figure (3).

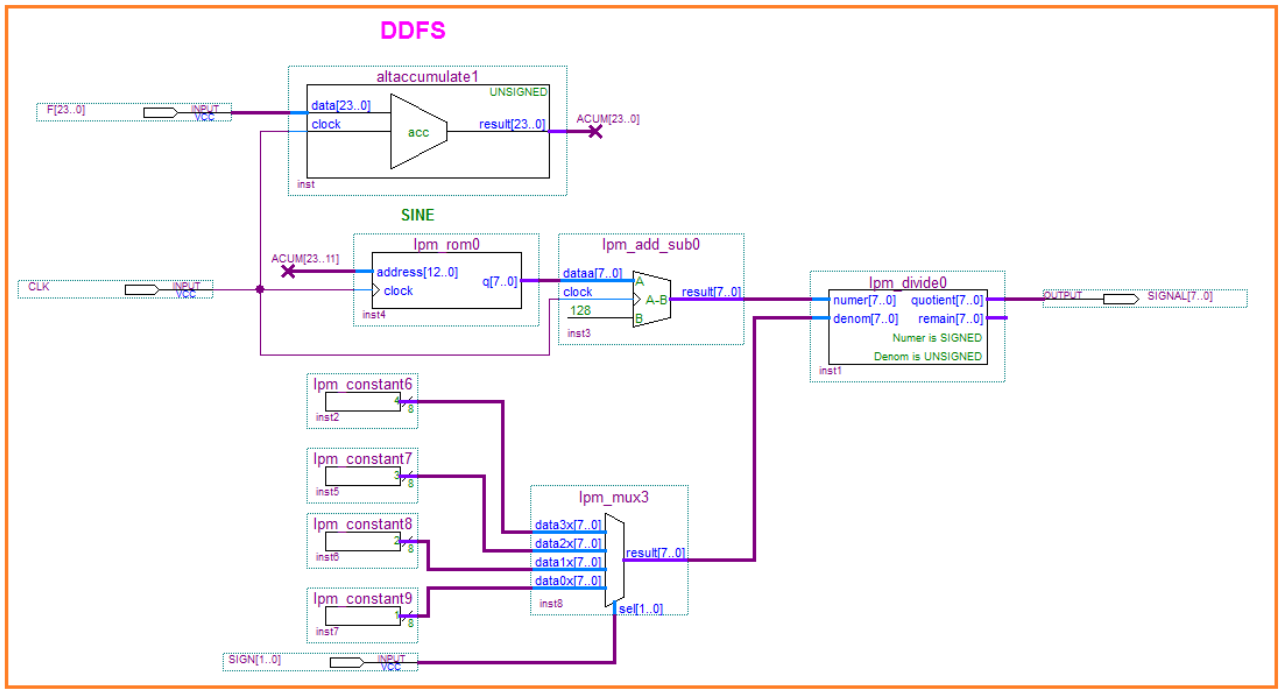

Fig (3): The block diagram of a DDFS in (Quartus II9.1)

VI. DESIGN OF THE DIGITAL PSEUDO-NOISE GENERATOR (DPNG) USING QUARTUS II 9.1

This signal is of white noise type and has an amplitude equals to 100% , 200% ,300% ,400% from the square pulse and sinusoidal signals amplitude, and it exists within the filter pass bands.

To generate the white noise signal, a digital pseudo noise generator DPNG is used, which consists of a shift register of k=60 bits and clock pulses of frequency equals to sampling frequency of 50MHz with maximum periodic time (T_{DPNG}) for the generated series [7]:

$$D_{DPNG} = (2^{K} - 1)\ T_{SAM} \qquad (4)$$

$$FOR\ K = 60\ , T_{SAM} = 0.02\ \mu S \Rightarrow$$

$$T_{DPNG} = (2^{60} - 1)\ X\ 0.02\ X\ 10^{-6} = 2.3\ X\ 10^{10}\ S$$

Or:

$$T_{DPNG} = \frac{2.3\ X\ 10^{10}\ S}{(3600\ X\ 24\ X\ 365)} = 731.2\ \ Year$$

Where K the number of shift register bits.
According to the diagram shown in figure (4), which consists of the following parts:
-Shift register of 60 bits and clock pulses with sampling frequency of 50MHz.
-Feedback circuit by using XOR gate and NOT gate.
The figure (5) shows the formed noise signal.

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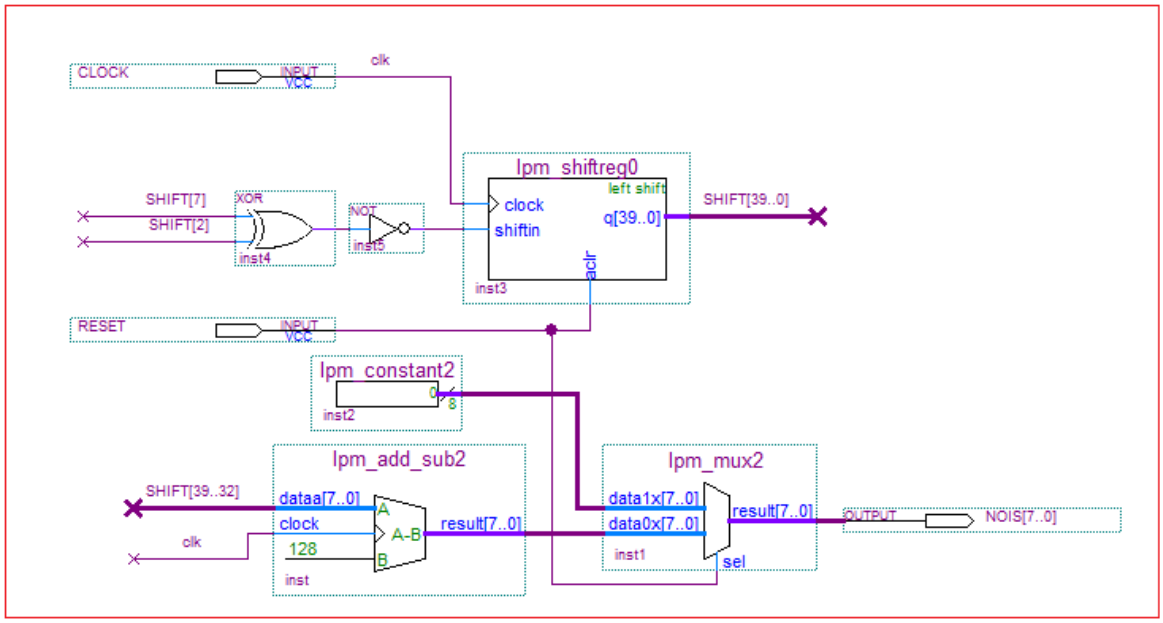

Fig. (4) The digital pseudo noise generator (DPNG) diagram

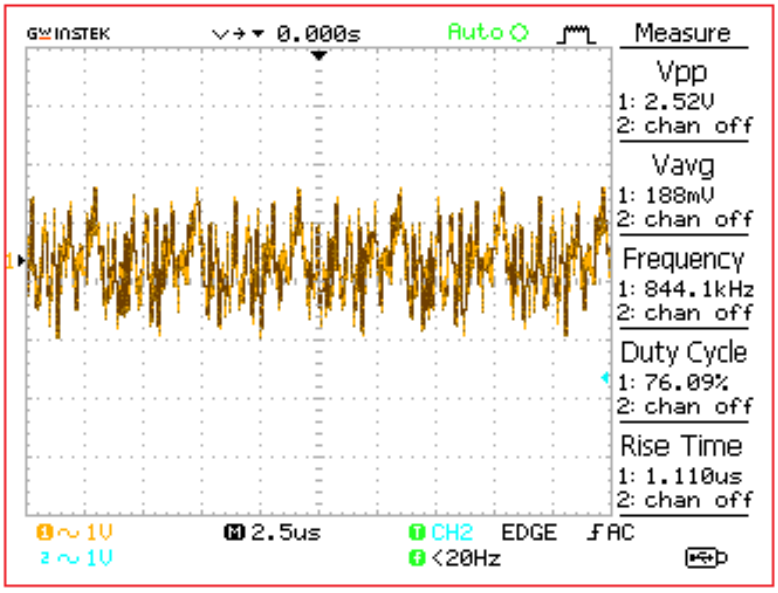

Fig. (5) The white noise signal of fsam =50MHz on the oscilloscope screen

VII. DESIGN OF THE DIGITAL MOVING AVERAGE FILTER USING QUARTUS II 9.1

The FIR digital smoothing filter (MAF) was designed using MATLAB and VHDL with the following parameters :

-Type of filter: MAF.
- Filter structure: Direct form - FIR
-Filter order: 512.
-Filter length: 513.
-$(SNR)_{inp}$ =(1/1 , 1/2 , 1/3 , 1/4) .
-Sampling frequency: fsam=50 MHz.
-Frequencies of input signals: finp=1 KHz.
-Word length: 8 bits.

The block diagram of the digital MAF designed in (Quartus II9.1) environment is shown in figure (6).

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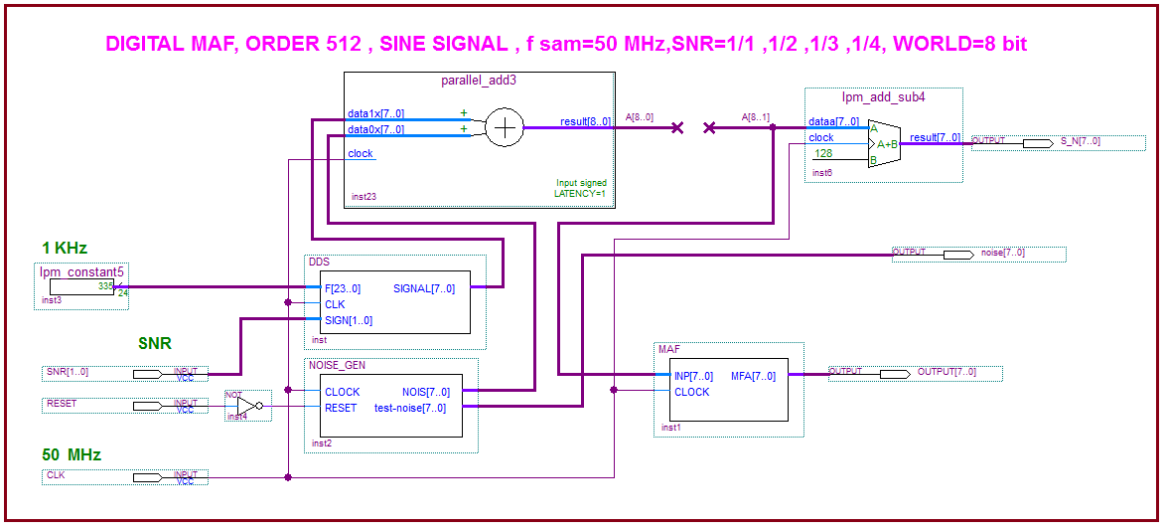

Fig (6): The block diagram of a digital MAF in (Quartus II9.1)

VIII. RESULTS OF DESIGN

The results of the practical design of the digital MAF for different cases (finp=1 KHz , $(SNR)_{inp}$ =(1/1) and sinusoidal and square signals) in time domain are shown in figure (7). The results of the practical design of the digital MAF for the difference case of $(SNR)_{inp}$ =(1/1 , 1/2 , 1/3 , 1/4) , difference case of filter order (32 , 128 , 512), sinusoidal and square signals are shown in figure (8), figure (9), and figure (10) . These figures are taken from the screen of digital oscilloscope. We notice from these figures the identification between the theoretical results and the practical results, which indicate the high accuracy of digital synthesizing and filtering operations[8].

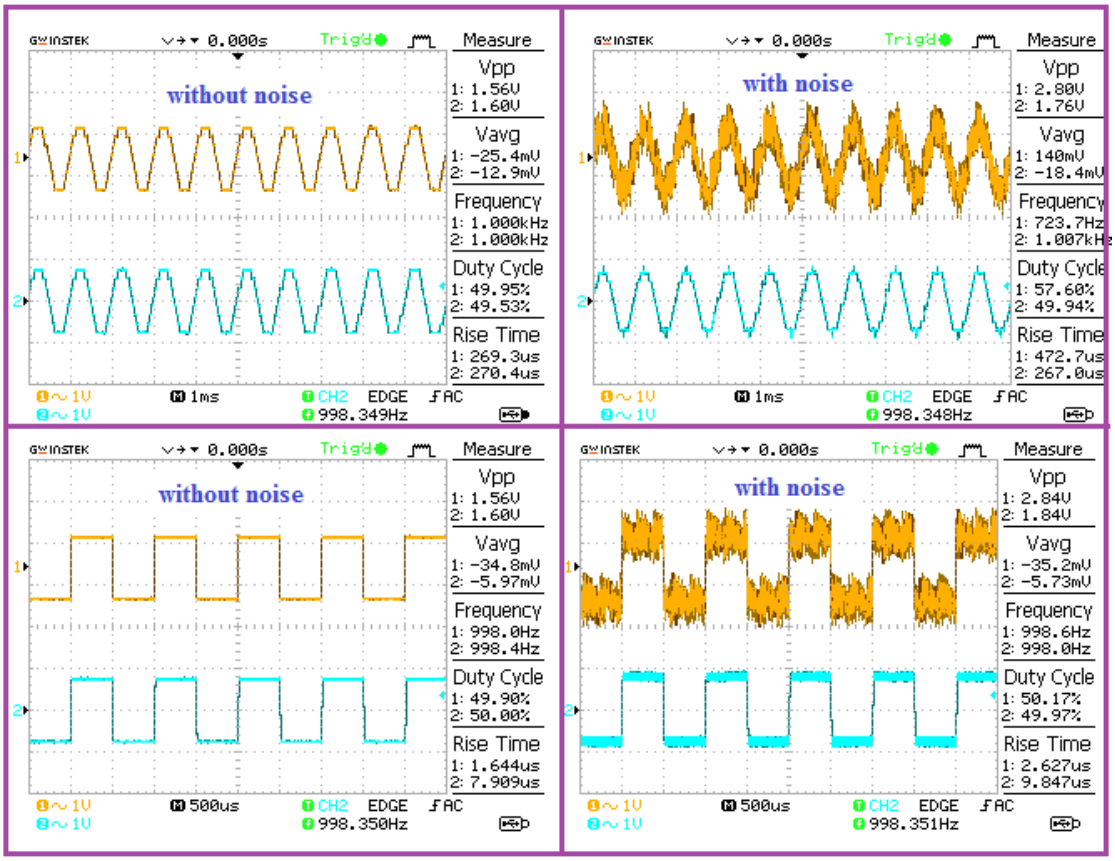

Fig. (7): The input and output signals of MAF for finp=1 KHz , filter order (512) for sinusoidal and square signals without noise and with noise for $(SNR)_{inp}$ =(1/1) in time domain.

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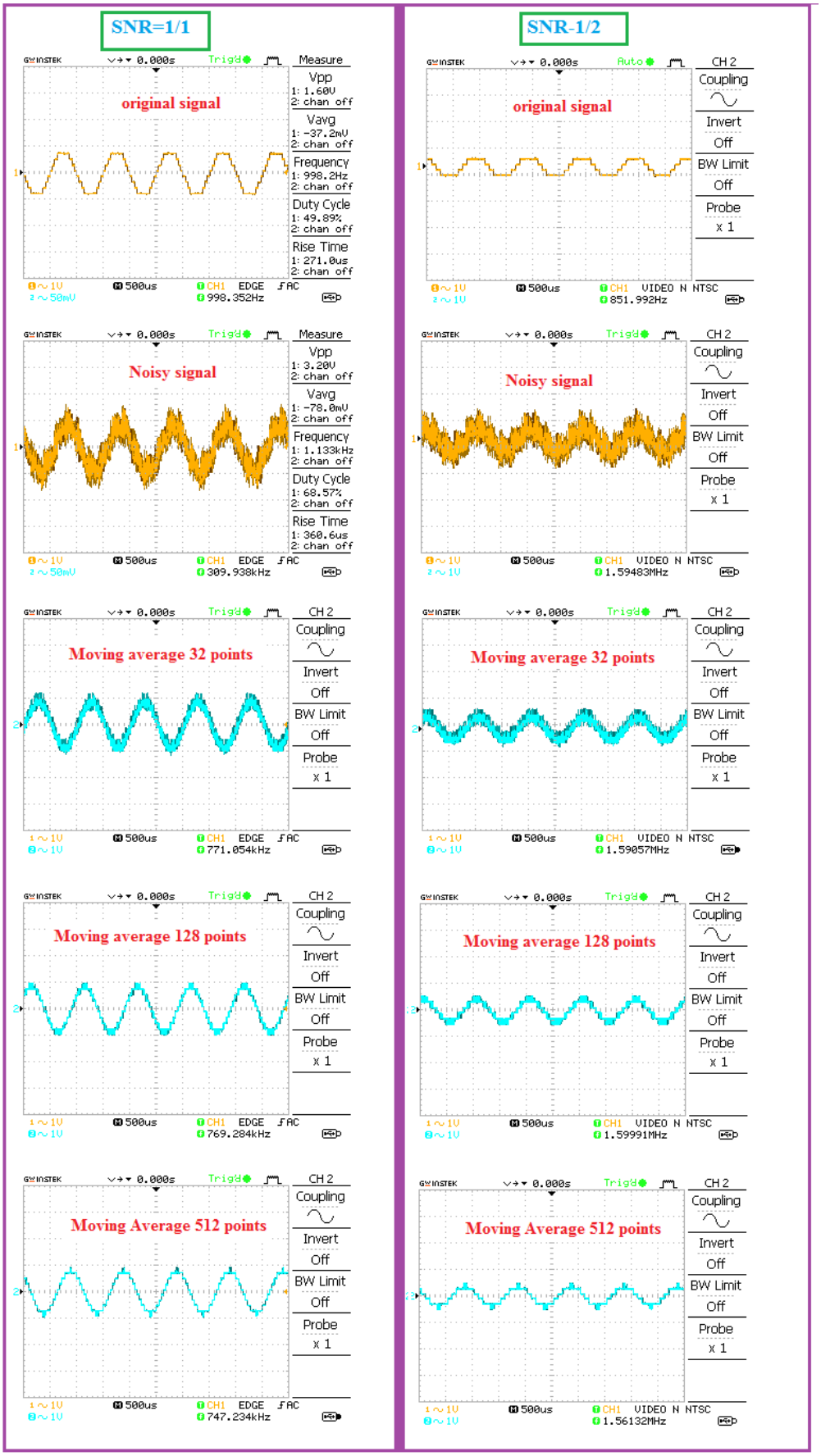

Fig. (8): The output signals of MAF for sinusoidal signal, finp=1 KHz , order (32, 128 ,512), ($SNR)_{inp}$ =(1/1) and $(SNR)_{inp}$ =(1/2) in time domain .

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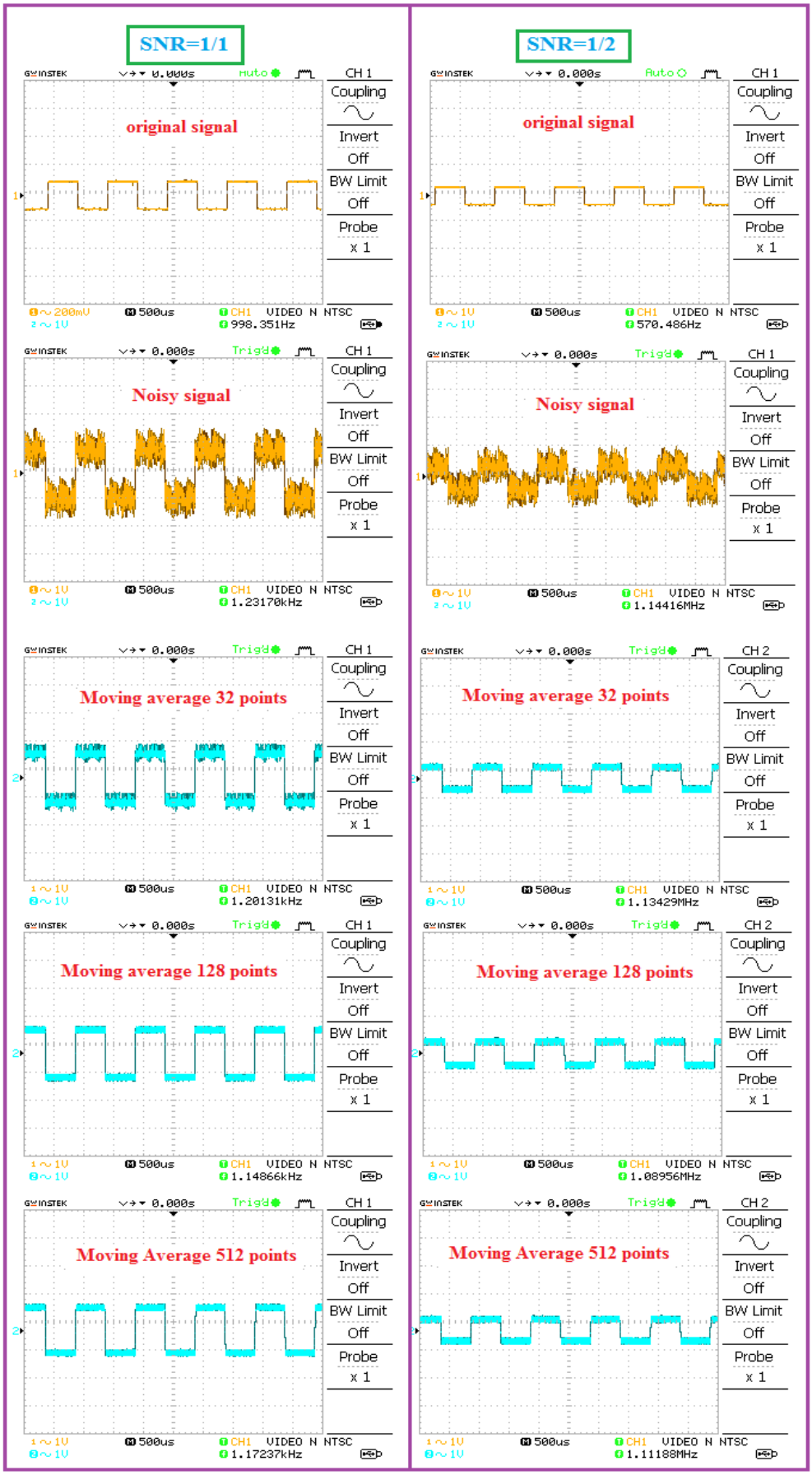

Fig. (9): The output signals of MAF for square signal, finp=1 KHz, order (32, 128 ,512), ($SNR)_{inp}$ =(1/1) and

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(SNR)$_{inp}$ =(1/2) in time domain .

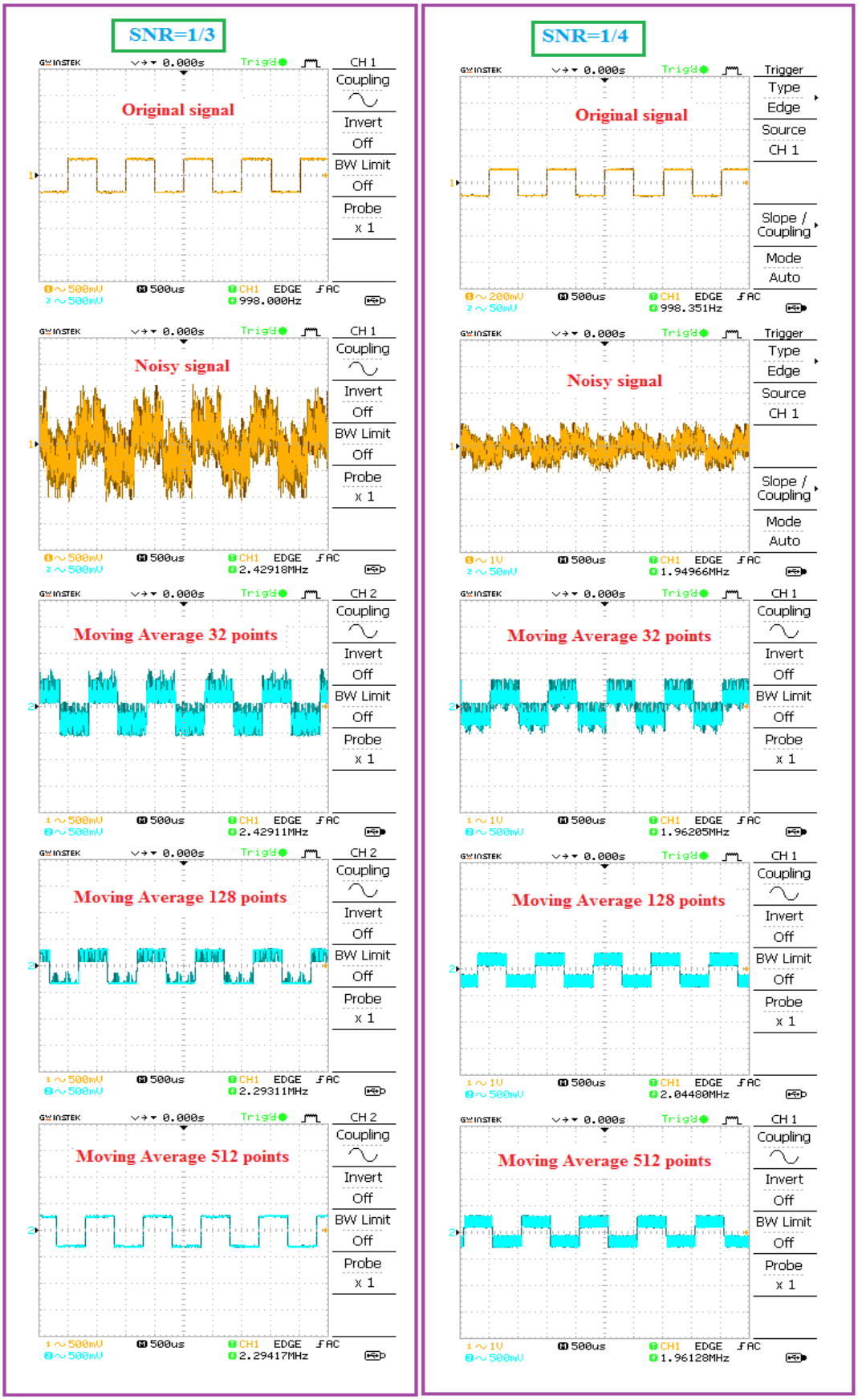

Fig. (10): The output signals of MAF for square signal, finp=1 KHz , order (32, 128 ,512), (SNR)$_{inp}$ =(1/3) and (SNR)$_{inp}$ =(1/4) in time domain .

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We notice from the former figures that the MAF filter reduced random noise while retained the sharp edge of the useful square signal, and the $(\mathrm{SNR})_{\mathrm{out}}$ improves as the filter order increases [9].

The values $(\mathrm{SNR})_{\mathrm{out}}$ for different filters orders are calculated according the following relation, and recorded in table (1)

$$(\mathrm{SNR})_{\mathrm{out}} = 10\log\left(\frac{N}{\sqrt{N}}\right) = 10\log\left(\sqrt{N}\right) \qquad (5)$$

Table (1)			
Values [SNR out] for deference filter orders $(\mathrm{SNR})_{\mathrm{out}} = 10\log\sqrt{N}$			
Filter Order	32	128	512
$(\mathbf{SNR})_{\mathbf{out}}$ **[dB]**	7.5	10.5	13.5

IX. DISCUSSION AND CONCLUSIONS

-Using digital filtering techniques in communication domain allows implementing different filters (LPF, HPF, PBF, BSF, MAF etc) with high accuracy and speed, and with the ability of changing parameters of signals in wide range.

-Using DDFS techniques in communication domain allows implementing the digital processing in the communication receiver on high intermediate frequency.

-We note from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital filtering for signals.

-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).

-The most important thing in this paper is the possibility of changing the frequency of the input signals.

- Moving average filter is effective to reduce random white noise, while keeping the sharpest step response.

-The performance or specifications of a digital filter can be improved by:

- Increasing the filter order.
- Increasing the number of bits of the input signal.
- Changing the window type.

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Working in the field of programming FPGA by using VHDL, and designing Digital Filters.

Dr. Maarouf Yousef: Holds a PhD in electrical engineering in 2001 from Egypt, technical engineering faculty. Holds assistant professor degree in 2009 from Aleppo university.

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