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Design and Implementation of a FIR Digital Band Stop Filter (BSF) using FPGA

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Abstract: Digital signal filtering is used in many different fields, including communications, radar, navigation and others, because of its excellent performance and the ability to obtain accurate results using FIR and IIR filters.
In this paper, we propose the design and implementation mechanism for FIR digital BSF based on the use of Cyclone II EP2C20F484C7 FPGA from ALTERA, placed on education and development board DE-1. The designed filter has the following parameters**:**
-Clock frequency: F_{CLK}=50 MHz.
-Sampling frequency: fsam= 2 MHz.
-Cut- off frequency of the band stop filter (BSF): fcut1=100 KHz , fcut2=200 KHz.
-Type of input signal is sinusoidal of frequency: finp1=50 KHz, finp2=100 KHz, , finp3=103 KHz , finp4=105 KHz , , finp5=150 KHz , finp6=200 KHz , finp7=203 KHz , finp8=205 KHz , finp9=250 KHz.
-The ROM capacity for the stored input signal samples is 8192X8 bits, and their values are positive within the range from
(0 to 255).
-Frequency range: (0.12 Hz…1 MHz).
-Frequency Resolution: (0.12 Hz).
- Signal amplitude (5V).
Digital designs using FPGA allow the system to be modified and developed to obtain better results through reprogramming according to the user's desire.

Keywords: digital filter, FIR, BSF, DDFS, FPGA.

I. INTRODUCTION

FPGA is considered as one of the distinctive tools for designing digital filters, because it contains a large number of logical elements. It is possible to design digital filters with a high order. Multi-shape windows can also be used to improve specifications of digital filter.
In this paper, we propose a new method to replace floating-point coefficients with integer coefficients, which makes the filtering process parallel and fast, and reduces the memory capacity used to store the coefficients, and approaches the accuracy of the fractional coefficient case.
The coefficients of the designed FIR digital BSF h(n) are computed in (MATLAB) environment, and converted to signed values (-127,…,+127) with length (8) bits, then they are used in the filter design program by (VHDL) language, where the digital convolution algorithm of the FIR digital BSF is implemented for impulse response samples of length (N=201) as shown in figure (1) , where(Z^{-1}) represents a digital delay line of length (8) bits, and a delay time equal to sampling pluses period (Tsam=0.5usec). This digital BSF is designed by (VHDL) [1] with (Quartus II9.1) programming environment according to the ideal frequency response shown figure (2).
reference [2] presents the Design and Implementation of Low-Pass, High-Pass and Band-Pass Finite Impulse Response (FIR) Filters Using FPGA, where filter order is 91, and filter band 30 KHz.

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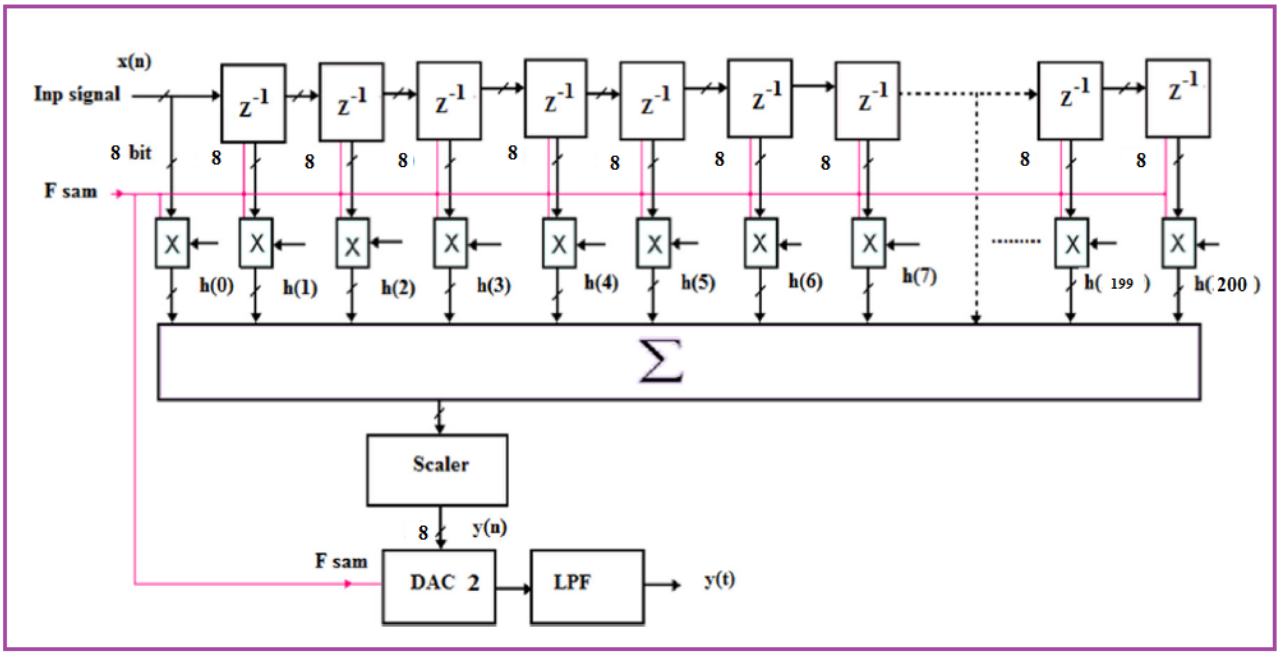

Fig. 1: The block diagram of the FIR digital filter

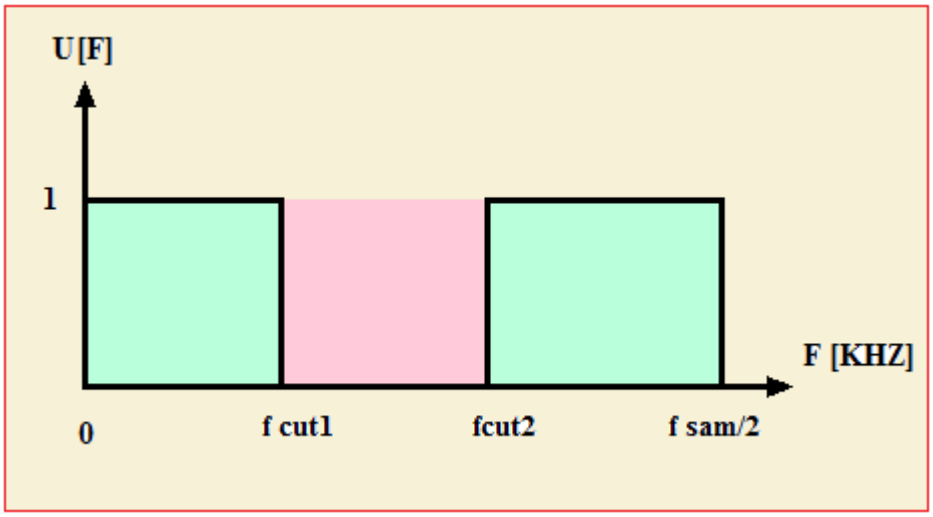

Fig. 2: The ideal frequency response of the digital BSF.

II. RESERCH IMPORTANCE AND ITS OBJECTIVES

-In this paper, FIR digital BSF was designed, implemented and tested based on the use of FPGA, VHDL and Graphical programming language of Quartus II 9.1 design environment.
-Using the digital convolution with mathematical operations (shifting, adding, multiply, division), makes the digital filters design process flexible, accurate and highly efficient.
-Changing the parameters of input signal (frequency), windows type, and filters order explains the difference between digital filters and analog filters.

III. RESERCH MATERIALS AND ITS WAYS

The following tools and software are used to design, and test digital filters of different types (LPF, HPF, BPF, BSF), different window types, and different values of input signals:
-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].

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-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment.
-Design Environment MATLAB.
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [4] shown in figure (3).

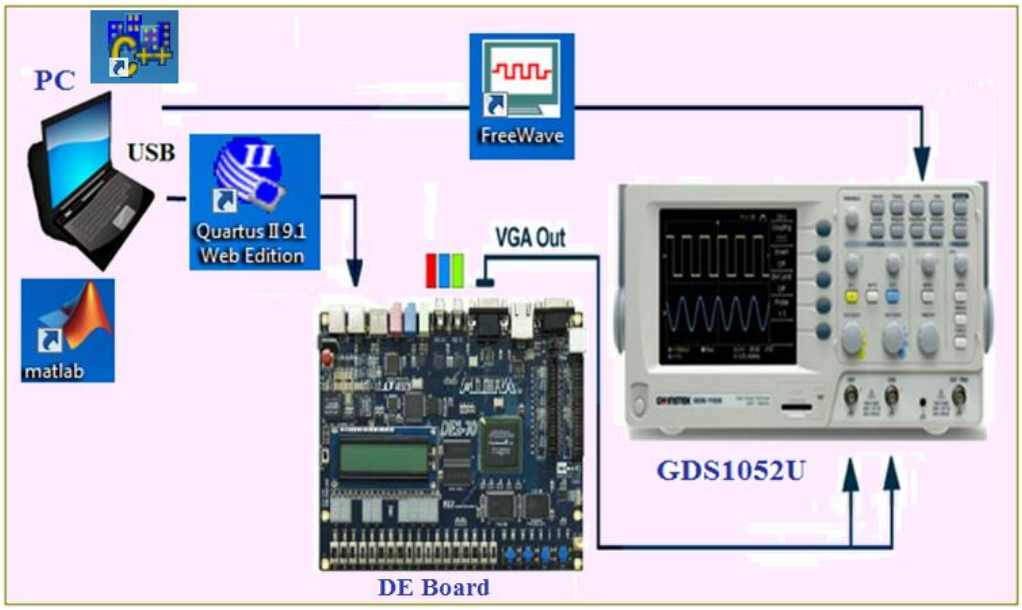

Fig (3): Block diagram of the laboratory experiment platform

IV. FILTERING ALGORITHM

The FIR digital filter output signal can be represented according to the following convolution relationship [5]:

$$y(n) = h(n) * x(n) = \sum_{k=0}^{N-1} h(k).x(n-k) \qquad (1)$$

Where: *x(n)* is the input signal samples in digital form.

N is number of samples for impulse response of the filter.

n is the sample number for input and output signals.

h(n) is the impulse response samples for digital filter, and it is given to BSF according to the following relationship [6]:

$$a_0 = h(0) = 1 - 2\frac{f_{cut2} - f_{cut1}}{f_{sam}} \quad , \quad for\ k = 0 \qquad (2)$$

$$a_k = h(k) = \frac{1}{\pi k}\left\{sin\left(2\pi k\ \frac{f_{cut1}}{f_{sam}}\right) - \sin\left(2\pi k\frac{f_{cut2}}{f_{sam}}\right)\right\} \quad , \quad for\ k \neq 0 \qquad (3)$$

Where:

$$n = 0, \ldots\ldots, N-1$$

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$$-\frac{(N-1)}{2} \leq k \leq \frac{(N-1)}{2} \quad (4)$$

For N=201:

$$-\frac{(N-1)}{2} \leq k \leq \frac{(N-1)}{2} \Rightarrow -100 \leq k \leq 100$$

$$h_{nor}(k) = \frac{h(k)}{h_{MAX}(k)} \quad (5)$$

$$h_{int}(k) = INT[127 * h_{nor}(k)] \quad (6)$$

Where:

$h_{nor}(k)$ Relative value, $h_{MAX}(k) = 0.9$ Maximum value, $h_{int}(k)$ Integer value.
The values of $h(k)$ are calculated using the MATLAB environment, Toolboxes-Filter Design-Filter Design & Analysis Tool (fdatool) , and then $h_{nor}(k)$, $h_{MAX}(k)$, $h_{int}(k)$ are recalculated according to the relationships (5) ,(6) and recorded in table (1).:

Table (1)

n	0	1	2	3	4	5	6	7	8
k=n-100	-100	-99	-98	-97	-96	-95	-94	-93	-92
h(k)	0	0.000896	0.001179	0.000466	0.0012045	-0.003350	0.0052109	0.0060241	-0.005324
h_{nor}(k) = h(k)/ h_{max}(k)	0	0	0	0	0	0	-0.005789	-0.006693	0.005916
h_{int}(k)= INT[127* h_{nor} (k)]	0	0	0	0	0	0	-1	-1	-1

.....

n	92	93	94	95	96	97	98	99	100
k=n-100	-8	-7	-6	-5	-4	-3	-2	-1	0
h(k)	0.061228	0.080035	0.081638	0.063662	0.028908	-0.015071	-0.057816	-0.0887346	0.9
h_{nor}(k) = h(k)/ h_{max}(k)	0.068031	0.88928	0.090709	0.070736	0.032120	-0.016745	-0.064240	-0.098594	1
h_{int}(k)= INT[127* h_{nor} (k)]	9	11	12	9	4	-2	-8	-13	127

.....

n	192	193	194	195	196	197	198	199	200
k=n-100	92	93	94	95	96	97	98	99	100
h(k)	0.005324	-0.006024	-0.005211	0.003351	-0.001204	0.000466	0.001179	0.000896	0
h_{nor}(k) = h(k)/ h_{max}(k)	0.005916	-0.006694	-0.005790	0.003723	-0.001457	0.000518	0.001311	0.000996	0
h_{int}(k)= INT[127* h_{nor} (k)]	-1	-1	-1	0	0	0	0	0	0

V. DESIGN OF THE DIGITAL FILTER USING MATLAB

The FIR digital band stop filter (BSF) was designed using MATLAB and VHDL with the following parameters [7]:
-Type of filter: BSF .
- Filter structure: Direct form - FIR
-Filter order: 200.
-Filter length: 201.
-Sampling frequency: 2MHz.
-Frequencies of input signals: finp1=50 KHz, finp2=100 KHz, , finp3=103 KHz , finp4=105 KHz , , finp5=150 KHz , finp6=200 KHz , finp7=203 KHz , finp8=205 KHz , finp9=250 KHz.

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-Cut-off frequency of BSF: fcut1=100 KHz, fcut2=200 KHz.
-Window type: Rectangular.
-Word length: 8 bits.
The specification and magnitude response of a digital filter designed in MATLAB is shown in figure (4).

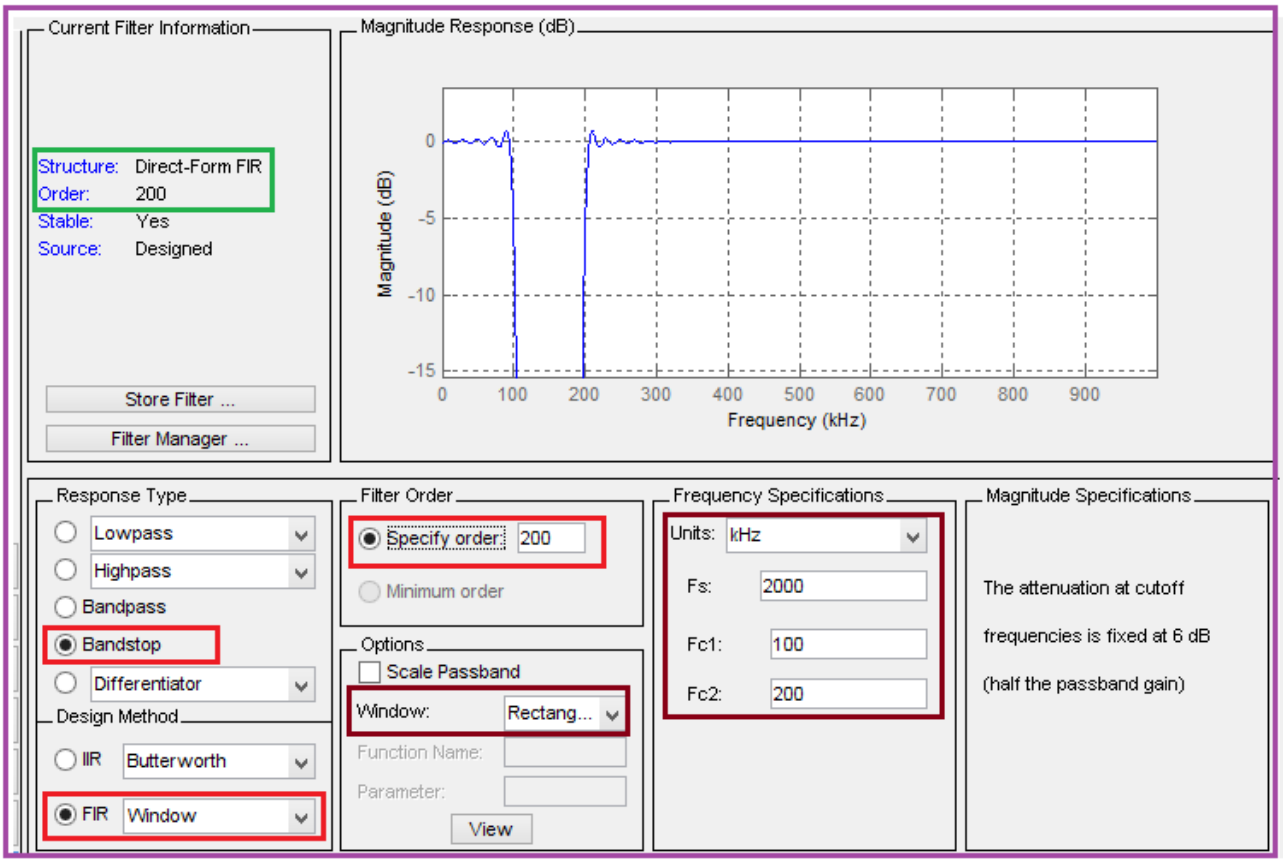

Fig (4): The specification and magnitude response of a digital filter designed in MATLAB

VI. DESIGN OF THE DDFS USIGN QUARTUS II 9.1

The designed DDFS has the following parameters:
-The frequency step i : $\delta f = 0.12\ Hz\ , and\ f_{sam} = 2\ MHz$.
-The input signal is sinusoidal of frequency finp1=50 KHz, finp2=100 KHz, , finp3=103 KHz , finp4=105 KHz , , finp5=150 KHz , finp6=200 KHz , finp7=203 KHz , finp8=205 KHz , finp9=250 KHz. and fsam= 2 MHz.
-The ROM capacity for the stored signal samples 8192X8 bits, and their values are positive within the range from 0 to 255.
-The number of the accumulator bits is computed from the following mathematical relation [8]:

$$\delta f = \frac{f_{sam}}{2^n} \qquad (7)$$

$$\delta f = \frac{f_{sam}}{2^n} \Longrightarrow 2^n = \frac{f_{sam}}{2^n} = \frac{2\ X\ 10^6}{0.12} \Longrightarrow n = 24\ \text{bits}$$

-The frequency range for the DDFS is computed from the following mathematical relation:

$$\Delta f = \delta f \ldots . \frac{f_{sam}}{2} = 0 \ldots . 1\ MHz$$

- The frequency code is calculated according the following relation [9]:

$$Code\ f = L = \frac{f.2^n}{f_{sam}} \qquad (8)$$

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So to synthesize nine input signals of frequencies finp1=50 KHz, finp2=100 KHz, , finp3=103 KHz , finp4=105 KHz , , finp5=150 KHz , finp6=200 KHz , finp7=203 KHz , finp8=205 KHz , finp9=250 KHz, finp9=250 KHz and fsam= 2 MHz, the frequency code of each one will be:

$$Code\ f_{sam} = L_{sam} = \frac{f_{sam}.\ 2^{n}}{F_{CLK}} = \frac{2X\ 2^{24}}{50} = 671089$$

$$Code\ f_{inp1} = L_{inp1} = \frac{f_{inp1}.\ 2^{n}}{f_{sam}} = \frac{0.050X\ 2^{24}}{2} = 419430$$

$$Code\ f_{inp2} = L_{inp2} = \frac{f_{inp2}.\ 2^{n}}{f_{sam}} = \frac{0.100X\ 2^{24}}{2} = 388861$$

$$Code\ f_{inp3} = L_{inp3} = \frac{f_{inp3}.\ 2^{n}}{f_{sam}} = \frac{0.103X\ 2^{24}}{2} = 864027$$

$$Code\ f_{inp4} = L_{inp4} = \frac{f_{inp4}.\ 2^{n}}{f_{sam}} = \frac{0.105X\ 2^{24}}{2} = 880804$$

$$Code\ f_{inp5} = L_{inp5} = \frac{f_{inp5}.\ 2^{n}}{f_{sam}} = \frac{0.150X\ 2^{24}}{2} = 1258291$$

$$Code\ f_{inp6} = L_{inp6} = \frac{f_{inp6}.\ 2^{n}}{f_{sam}} = \frac{0.200\ X\ 2^{24}}{2} = 1677722$$

$$Code\ f_{inp7} = L_{inp7} = \frac{f_{inp7}.\ 2^{n}}{f_{sam}} = \frac{0.203\ X\ 2^{24}}{2} = 1702887$$

$$Code\ f_{inp8} = L_{inp8} = \frac{f_{inp8}.\ 2^{n}}{f_{sam}} = \frac{0.205\ X\ 2^{24}}{2} = 1719665$$

$$Code\ f_{inp9} = L_{inp9} = \frac{f_{inp9}.\ 2^{n}}{f_{sam}} = \frac{0.250\ X\ 2^{24}}{2} = 2097152$$

The block diagram of the digital BSF designed in (Quartus II9.1) environment is shown in figure (5).

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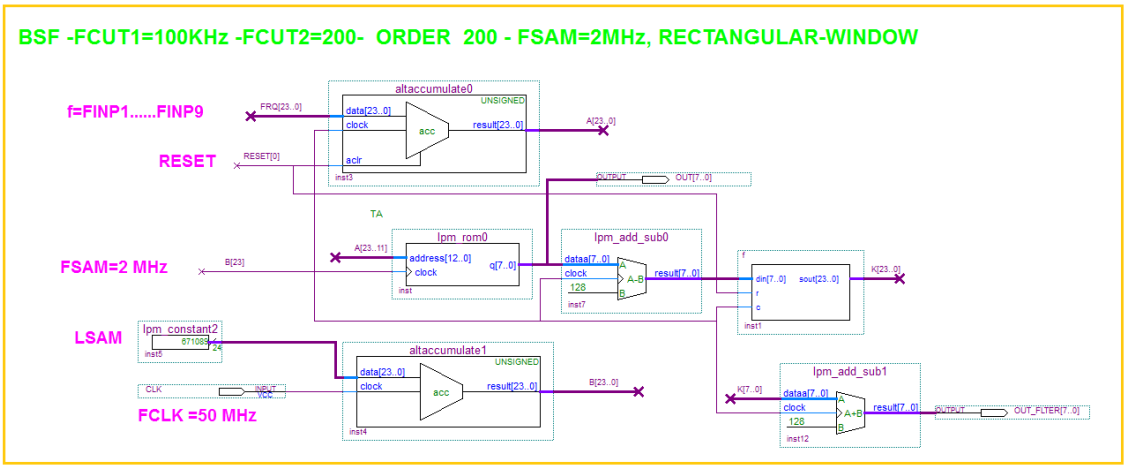

Fig (5): The block diagram of a digital BSF in (Quartus II9.1)

VII. RESULTS OF DESIGN

The results of the practical design of the digital BSF for different cases (finp1=50 KHz, finp2=100 KHz, , finp6=200 KHz, finp9=250 KHz.) in time domain are shown in figure. (6). The results of the practical design of the digital BSF for the same previous cases in frequency domain are shown in figure (7), figure (8), figure (9), figure (10), and figure (11). These figures are taken from the screen of digital oscilloscope, and digital spectrum analyzer. We notice from these figures the identification between the theoretical results and the practical results, which indicate the high accuracy of digital synthesizing and filtering operations.

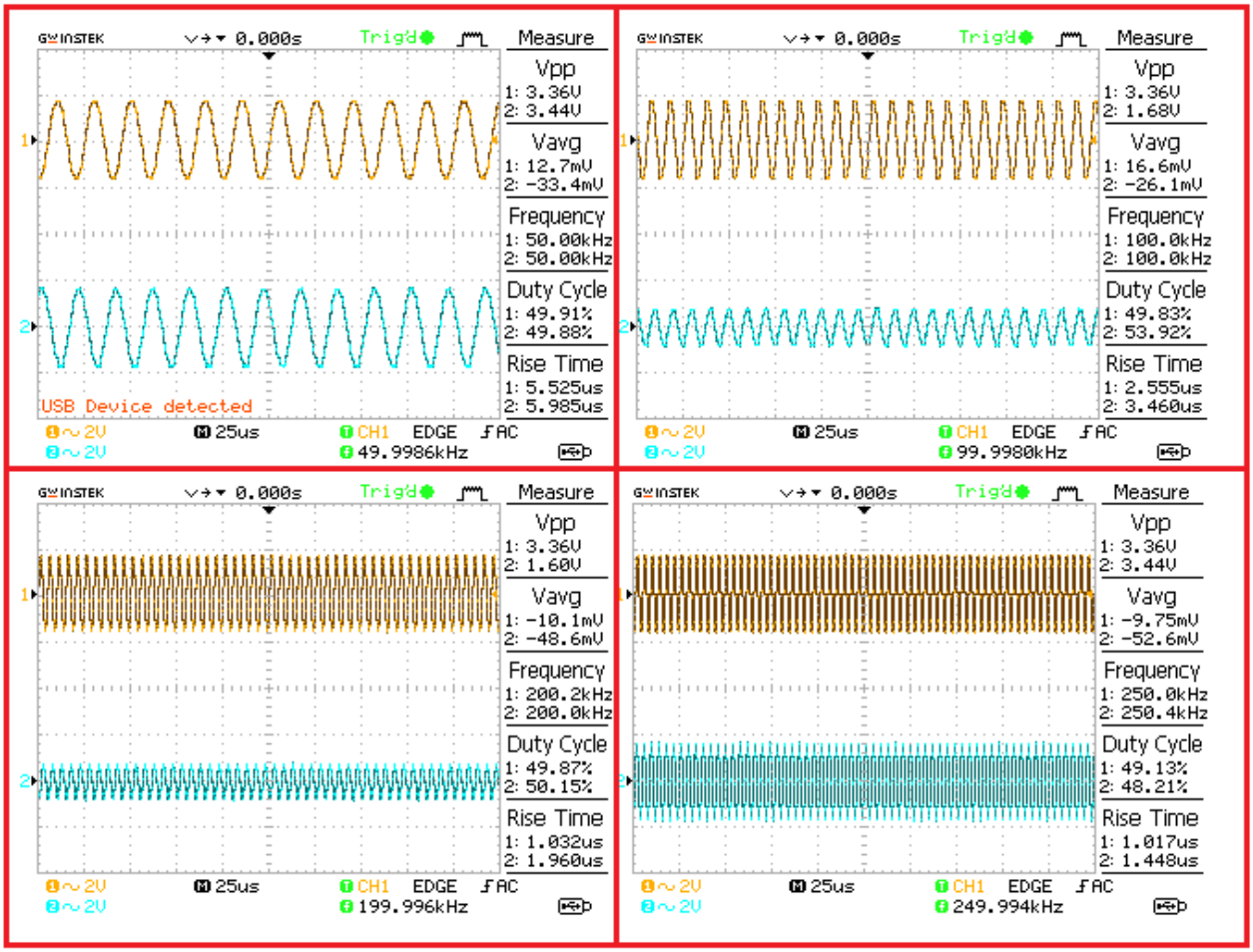

Fig. (6): The input and output signals of BSF for finp1=50 KHz, finp2 =100 KHz , finp6=200 KHz and finp9=250 KHz in time domain.

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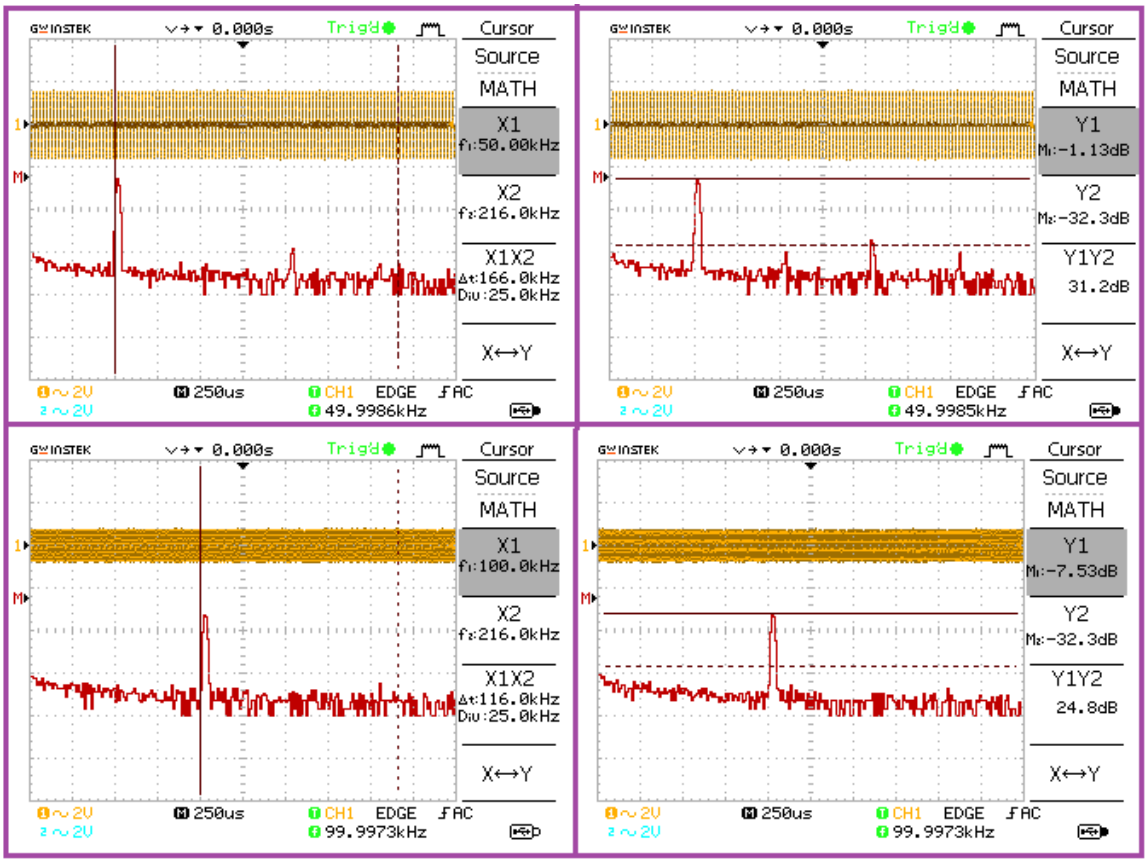

Fig. (7): The output signals for finp1=50 and finp2=100 KHz in frequency domain.

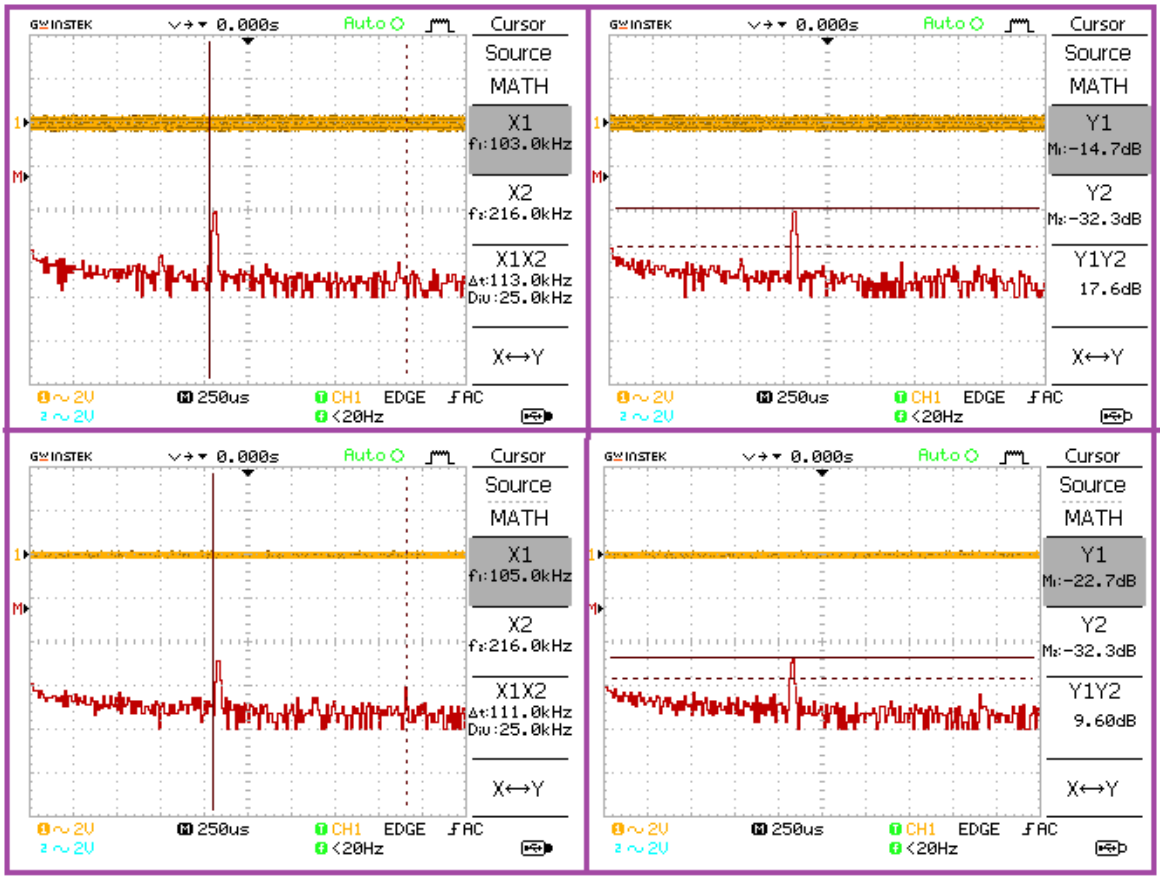

Fig. (8): The output signals for finp3=103 KHz and finp4=105 KHz in frequency domain

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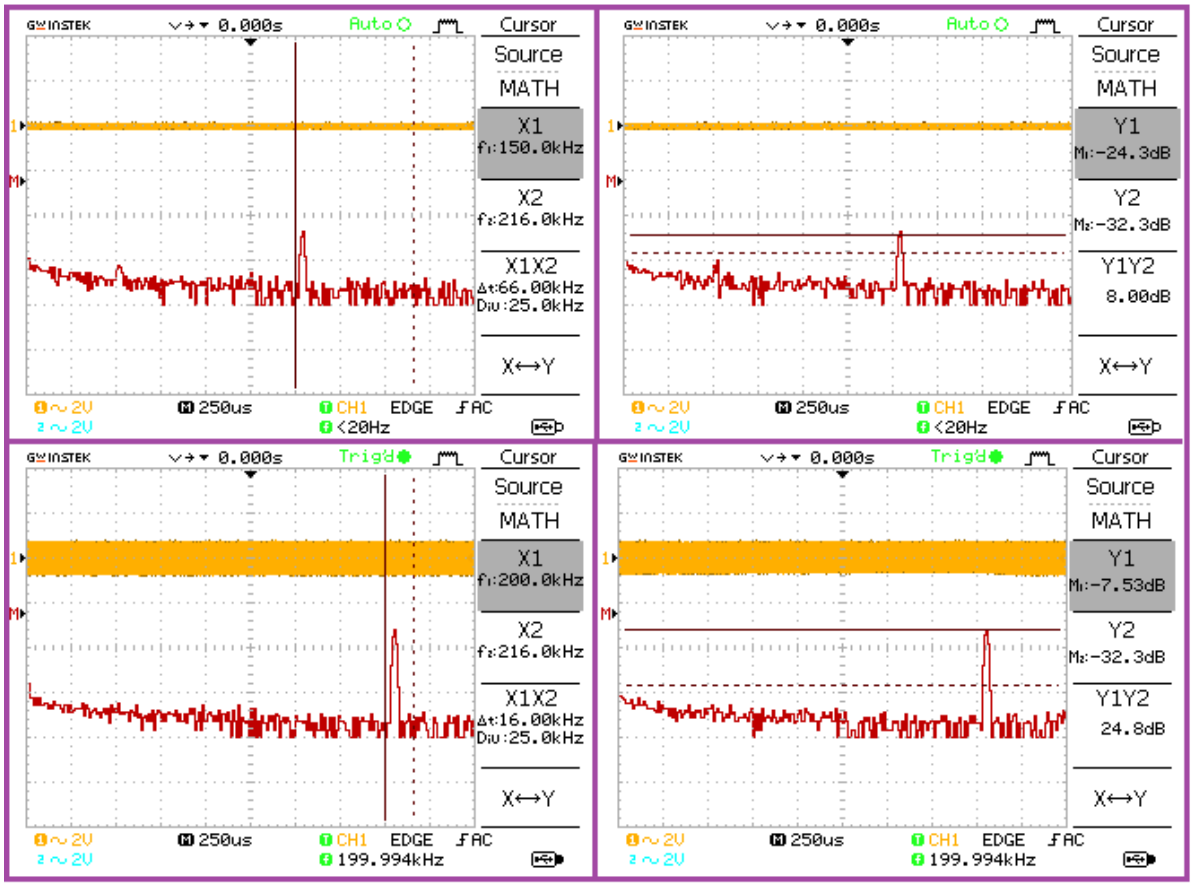

Fig. (9): The output signals for finp5=150 KHz and finp6=200 KHz in frequency domain

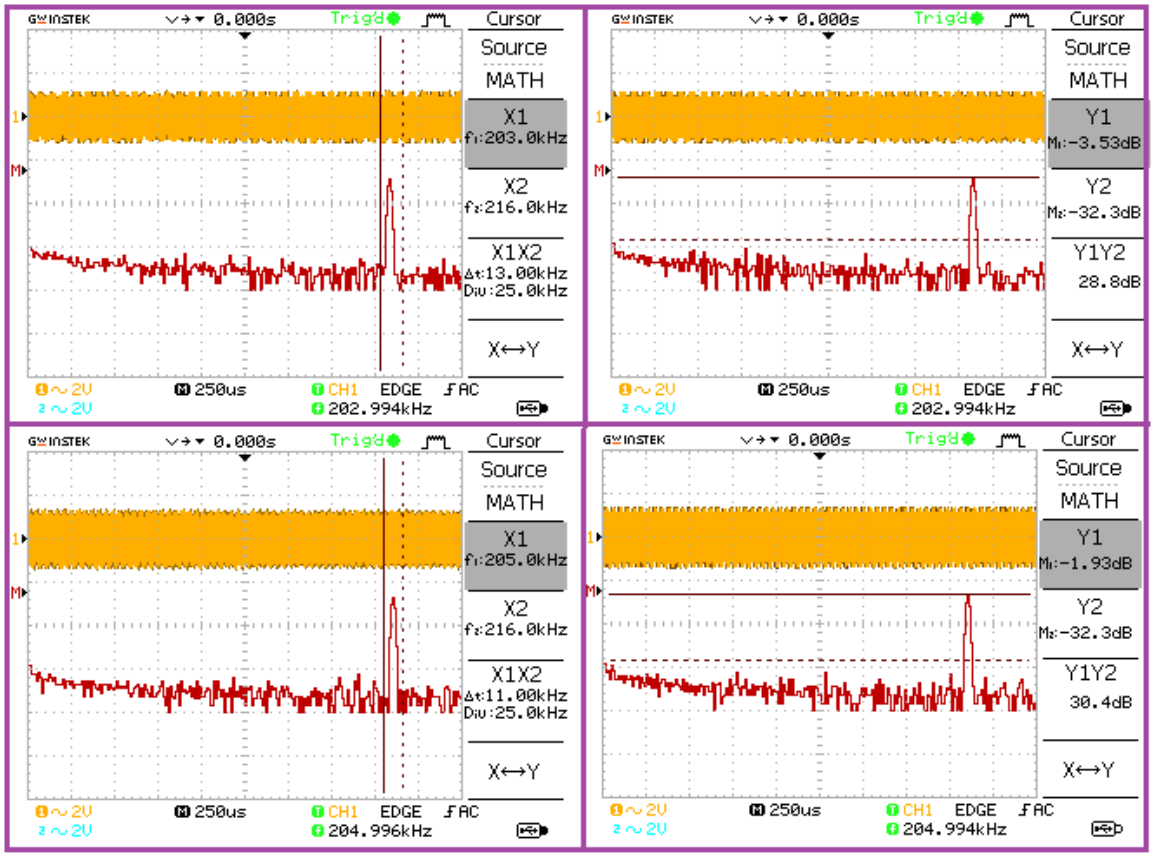

Fig. (10): The output signals for finp7=203 KHz and finp8=205 KHz in frequency domain

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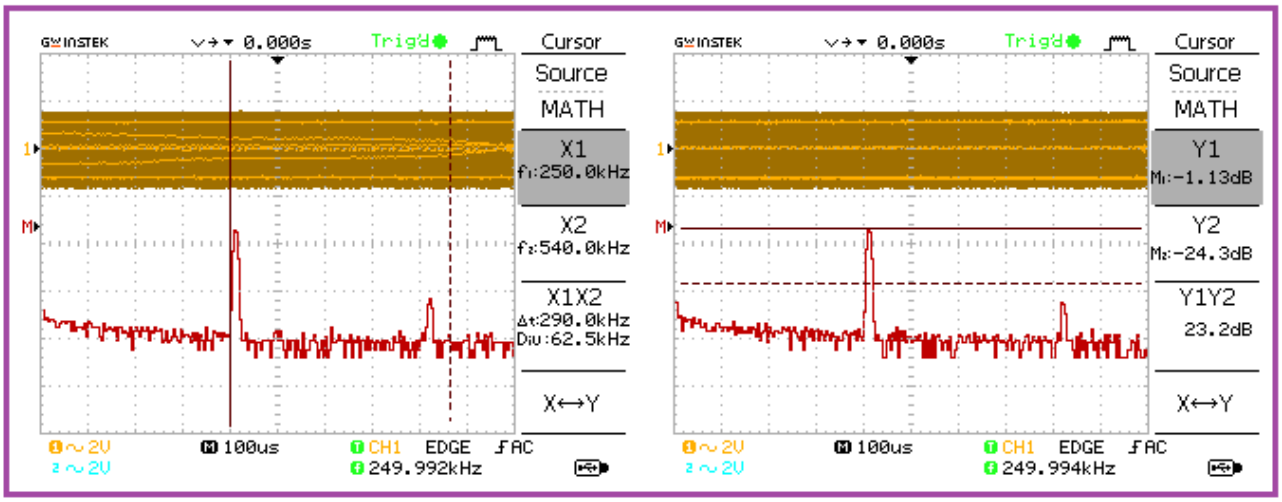

Fig. (11): The output signals for finp9=250 KHz in frequency domain

The values [Uout] for different input frequencies are recorded in table (2).

Table (2).

Values [Uout] For Deference Frequency

Frequency	**finp1**	**finp2**	**finp3**	**finp4**	**finp5**	**finp6**	**finp7**	**finp8**	**finp9**
f inp[KHZ]	50	100	103	105	150	200	203	205	250
Uout [dB]	-1.13	-7.53	-14.7	-22.7	-24.3	-7.53	-3.53	-1.93	-1.13
Uout{*FOR* f = 105} − Uout{*FOR* f = 50} =−24. 3 − (−1. 13) = - 23.17 dB									

The frequency response of the designed digital BSF is shown in figure (12).

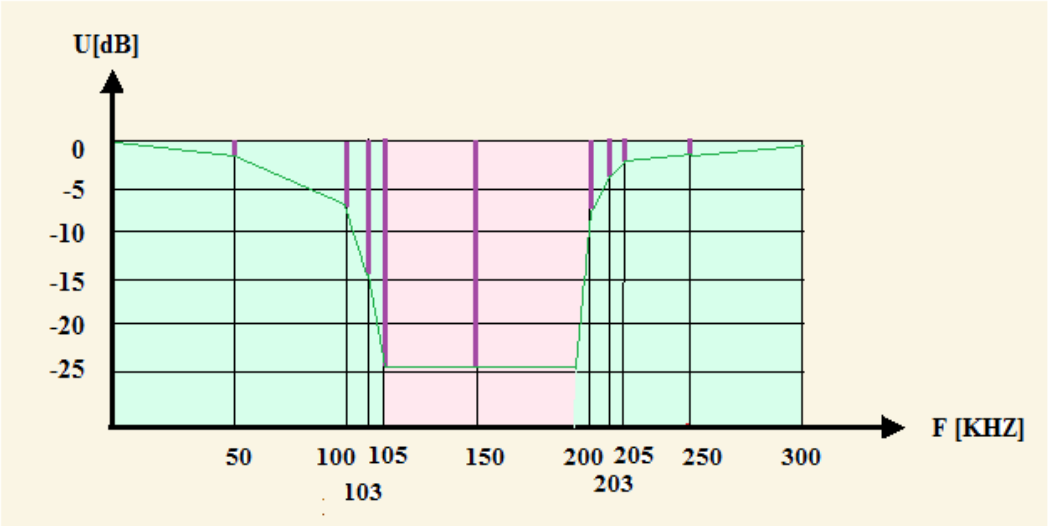

Fig. (12): The frequency response of the designed digital BSF

From the figures we notice that the designed BSF works correctly (passes the signal of frequencies (0-100KHz) , (200-1000KHz) and suppresses the signal of frequencies (100-200KHz).

VIII. DISCUSSION AND CONCLUSIONS

-Using digital filtering techniques in communication domain allows implementing different filters (LPF, HPF, BPF, BSF etc) with high accuracy and speed, and with the ability of changing parameters of signals in wide range.
-Using DDFS techniques in communication domain allows implementing the digital processing in the communication receiver on high intermediate frequency.
-We note from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital filtering for signals.

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-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).
-The most important thing in this paper is the possibility of changing the frequency of the input signals.
-The performance or specifications of a digital filter can be improved by:
- Increasing the filter order.
- Increasing the number of bits of the input signal.
- Changing the window type.

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BIOGRAPHY

Dr. Kamal Aboutabikh: Holds a PhD in communication engineering in 1988 from the USSR, university of communication in Leningrad. Holds assistant professor degree in 2009 from Aleppo university.
Lecturer at Department of Biomedical Engineering, Al Andalus University For Medical Sciences-Syria. Lecturer at Tishreen University-Syria, and Corduba Private University- Syria. Former Lecturer at Kassala University-Sudan and Ittihad Private University- Syria.
Published a lot of researches in the field of digital communication, and digital signal processing in the university’s journals of Syria and in the European and Indian journals.
Working in the field of programming FPGA by using VHDL, and designing Digital Filters.

Dr. Maarouf Yousef: Holds a PhD in electrical engineering in 2001 from Egypt, technical engineering faculty. Holds assistant professor degree in 2009 from Aleppo university.
Lecturer at electrical engineering faculty, Al Assad academy, Aleppo University -Syria.
Published a lot of researches in the field of digital signal processing, radar signal processing, GPS system. in the university’s journals of Syria.
Working in the fields of digital circuit design, and programming FPGA by using VHDL, digital signal processing.