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Design and Implementation of a FIR Digital Low Pass Filter (LPF) using FPGA

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Abstract
Digital signal filtering is used in many different fields, including communications, radar, navigation and others, because of its excellent performance and the ability to obtain accurate results using FIR and IIR filters.
In this paper, we propose the design and implementation mechanism for FIR digital LPF based on the use of Cyclone II EP2C20F484C7 FPGA from ALTERA, placed on education and development board DE-1. The designed filter has the following parameters**:**
-Clock frequency: F_{CLK}=50 MHz.
-Sampling frequency: fsam= 2 MHz.
-Cut- off frequency of the low pass filter (LPF): fcut=100 KHz.
-Type of input signal is: sinusoidal of frequency: finp1=50 KHz, finp2=100 KHz, finp3=102 KHz.
-The ROM capacity for the stored input signal samples is 8192X8 bits, and their values are positive within the range from
(0 to 255).
-Frequency range: (3 Hz…25 MHz).
-Frequency Resolution: (3 Hz).
-Signal amplitude (5V).
Digital designs using FPGA allow the system to be modified and developed to obtain better results through reprogramming according to the user's desire.

Keywords: digital filter, FIR, LPF, DDFS, FPGA.

I. INTRODUCTION

FPGA is considered as one of the distinctive tools for designing digital filters, because it contains a large number of logical elements. It is possible to design digital filters with a high order. Multi-shape windows can also be used to improve specifications of digital filter.

In this paper, we propose a new method to replace floating-point coefficients with integer coefficients, which makes the filtering process parallel and fast, and approaches the accuracy of the fractional coefficient case, and reduces the memory capacity used to store the coefficients.

The coefficients of the designed FIR digital LPF h(n) are computed in (MATLAB) environment, and converted to signed values (-127,…,+127) with length (8) bits, then they are used in the filter design program by (VHDL) language, where the digital convolution algorithm of the FIR digital LPF is implemented for impulse response samples of length (N=201) as shown in figure (1) , where(Z^{-1}) represents a digital delay line of length (8) bits and a delay time equal to sampling pluses period (Tsam=0.5usec). This digital LPF is designed by (VHDL) [1] with (Quartus II9.1) programming environment according to the frequency response shown figure (2).

reference [2] presents the Design and Implementation of Low-Pass, High-Pass and Band-Pass Finite Impulse Response (FIR) Filters Using FPGA, where filter order is 91, and filter band 30 KHz.

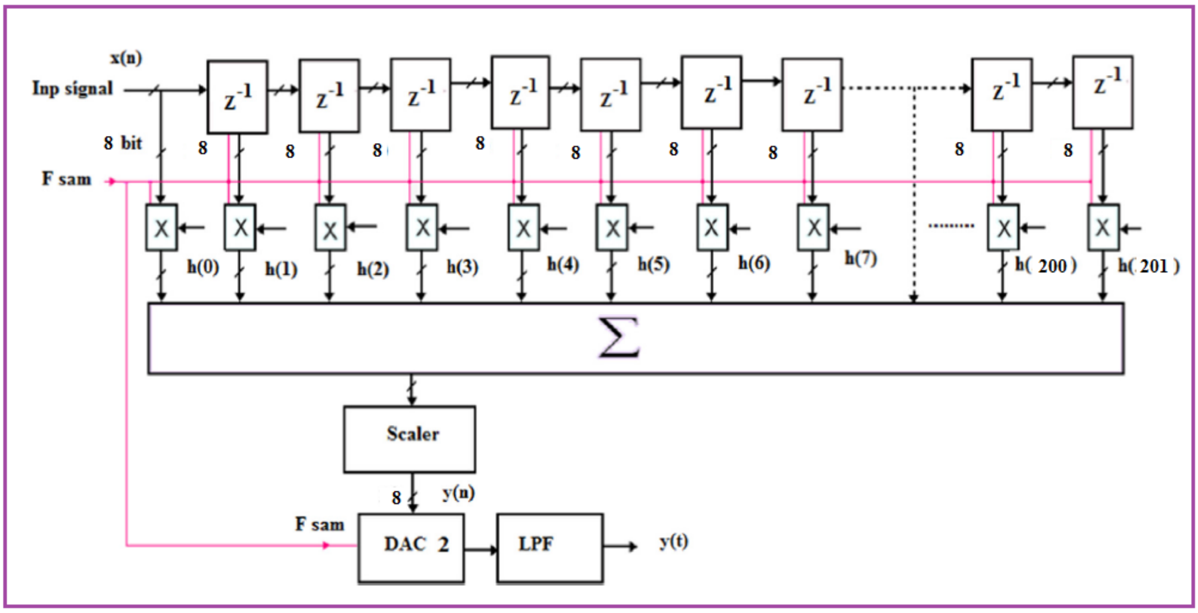


Fig. 1: The block diagram of the FIR digital filter

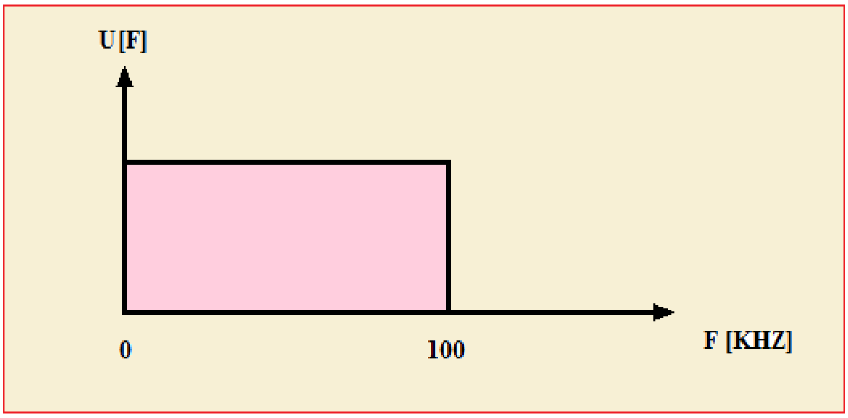


Fig. 2: The frequency response of the LPF

II. RESERCH IMPORTANCE AND ITS OBJECTIVES

-In this paper, FIR digital LPF was designed, implemented and tested based on the use of FPGA, VHDL and Graphical programming language of Quartus II 9.1 design environment.
-Using the digital convolution with mathematical operations (shifting, adding, multiply, division), makes the digital filters design process flexible, accurate and highly efficient.
-Changing the parameters of input signal (frequency), windows type, and filters order explains the difference between digital filters and analog filters.

III. RESERCH MATERIALS AND ITS WAYS

The following tools and software are used to design, and test digital filters of different types (LPF, HPF, BPF), different of window types, and different values of input signals:
-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].
-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment.
-Design Environment MATLAB.
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [4] is shown in figure (3).

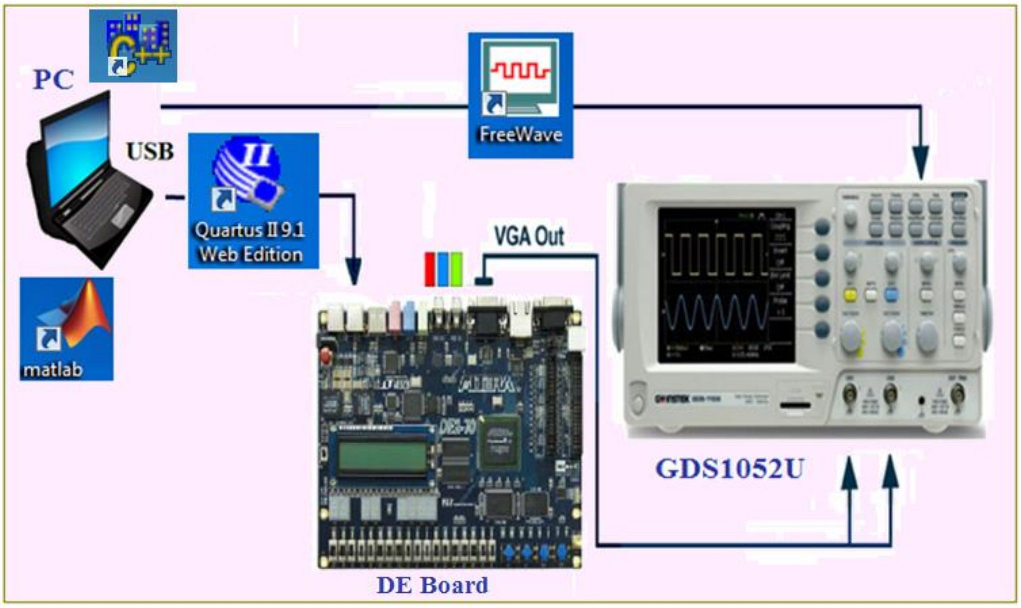


Fig (3): Block diagram of the laboratory experiment platform

IV. FILTERING ALGORITHM

The FIR digital filter output signal can be represented according to the following convolution relationship [5]:

$$y(n) = h(n) * x(n) = \sum_{k=0}^{N-1} h(k).x(n-k) \qquad (1)$$

Where: *x(n)* is the input signal samples in digital form.
N is number of samples for impulse response of the filter.
n is the sample number for input and output signals.
h(n) is the impulse response samples for digital filter and it is given to LPF according to the following relationship [6]:

$$a_0 = h(0) = 2\frac{f_{cut}}{f_{sam}} \quad , \quad for\ k = 0 \qquad (2)$$

$$a_k = h(k) = \frac{1}{\pi k} sin\left(2\pi k\ \frac{f_{cut}}{f_{sam}}\right) \quad , \quad for\ k \neq 0 \qquad (3)$$

Where:

$$n = 0, \dots \dots .., N-1$$

$$-\frac{(N-1)}{2} \leq k \leq \frac{(N-1)}{2} \qquad (4)$$

For *N*=201:

$$-\frac{(N-1)}{2} \leq k \leq \frac{(N-1)}{2} \Rightarrow -100 \leq\ k \leq +100$$

$$h_{nor}(k) = \frac{h(k)}{h_{MAX}(k)} \qquad (5)$$

$$h_{int}(k) = INT[127 *\ h_{nor}(k)\ ] \qquad (6)$$

Where:

$h_{nor}(k)$ Relative value, $h_{MAX}(k) = 0.1$ Maximum value, $h_{int}(k)$ Integer value.
The values $h_{nor}(k)$, $h_{int}(k)$ are calculated according to the previous mathematical (5), (6) relationships and recorded in the table (1).

Table (1)

n	0	1	2	3	4	5	6	7	8
k=n-100	-100	-99	-98	-97	-96	-95	-94	-93	-92
h(k)	0	-0.000994	-0.00191	-0.00266	-0.00315	-0.00335	-0.00322	-0.00277	-0.00203
$h_{nor}(k)$ = h(k)/ $h_{max}(k)$	0	-0.00994	-0.0191	-0.0266	-0.0315	-0.0335	-0.0322	-0.0277	-0.0203
$h_{int}(k)$= INT[127* $h_{nor}(k)$]	0	-1	-2	-3	-4	-4	-4	-4	-3

....

n	92	93	94	95	96	97	98	99	100
k=n-100	-8	-7	-6	-5	-4	-3	-2	-1	0
h(k)	0.02339	0.03679	0.05046	0.06366	0.07568	0.08539	0.09355	0.09836	0.1
$h_{nor}(k)$ = h(k)/ $h_{max}(k)$	0.2339	0.3679	0.5046	0.6366	0.7568	0.8539	0.9355	0.9836	1
$h_{int}(k)$= INT[127* $h_{nor}(k)$]	30	47	64	81	96	109	119	125	127

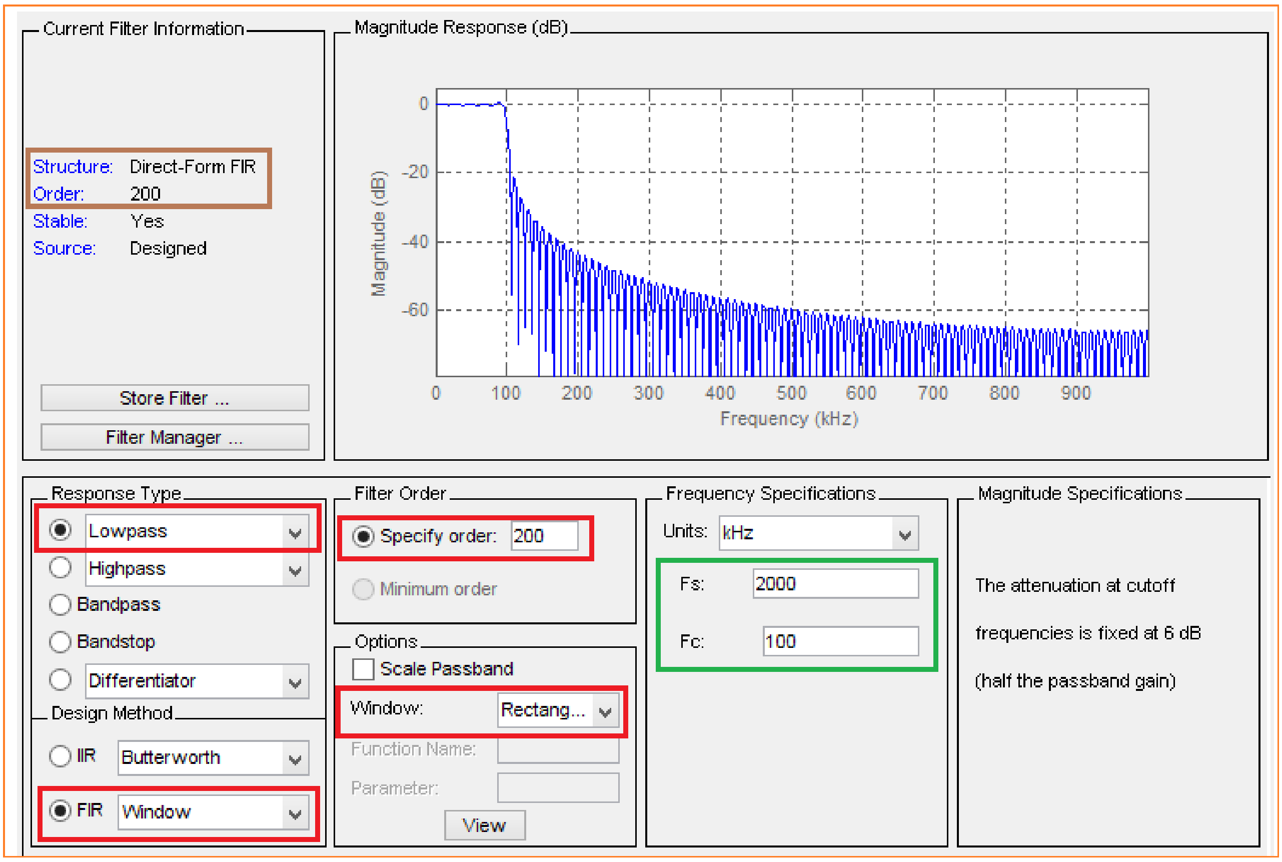
....

n	192	193	194	195	196	197	198	199	200
k=n-100	92	93	94	95	96	97	08	99	100
h(k)	-0.00203	-0.00277	-0.00322	-0.00335	-0.00315	-0.00266	-0.00191	-0.00099	0
$h_{nor}(k)$ = h(k)/ $h_{max}(k)$	-0.0203	-0.0277	-0.0322	-0.0335	-0.0315	-0.0266	-0.0191	0.0004	0
$h_{int}(k)$= INT[127* $h_{nor}(k)$]	-3	-4	-4	-4	-4	-3	-2	-1	0

V. DESIGN OF THE DIGITAL FILTER USING MATLAB

The FIR digital low pass filter (LPF) was designed using MATLAB and VHDL with the following parameters [7]:

-Type of filter: LPF.
- Filter structure: Direct form - FIR
-Filter order: 200.
-Filter length: 201.
-Sampling frequency: 2MHz.
-Frequencies of input signals: 50 ,100 ,102KHz.
-Cut-off frequency of LPF: 100 KHz.
-Window type: Rectangular.
-Word length: 8 bits.
The specification and magnitude response of a digital filter designed in MATLAB is shown in figure (4).



Current Filter Information

Structure: Direct-Form FIR
Order: 200
Stable: Yes
Source: Designed

Response Type
● Lowpass
○ Highpass
○ Bandpass
○ Bandstop
○ Differentiator

Design Method
○ IIR Butterworth
● FIR Window

Filter Order
● Specify order: 200
○ Minimum order

Options
□ Scale Passband
Window: Rectang...
Function Name:
Parameter:

Frequency Specifications
Units: kHz
Fs: 2000
Fc: 100

Magnitude Specifications
The attenuation at cutoff frequencies is fixed at 6 dB (half the passband gain)

Fig (4): The specification and magnitude response of a digital filter designed in MATLAB

VI. DESIGN OF THE DDFS USIGN QUARTUS II 9.1

The designed DDFS has the following parameters:
-The frequency step i : $\delta f = 3\ Hz$, and $F_{CLK} = 50\ MHz$.
-The input signal is sinusoidal of frequency finp1=50 KHz, finp2=100KHz, finp3=102 KHz, and fsam= 2 MHz.
-The ROM capacity for the stored signal samples 8192X8 bits and their values are positive within the range from 0 to 255.
-The number of the accumulator bits is computed from the following mathematical relation [8]:

$$\delta f = \frac{F_{CLK}}{2^n} \qquad (7)$$

$$\delta f = \frac{F_{CLK}}{2^n} \Longrightarrow 2^n = \frac{F_{CLK}}{\delta f} = \frac{50\ X\ 10^6}{3} = 24 \text{ bits}$$

-The frequency range for the DDFS is computed from the following mathematical relation:

$$\Delta f = 0 \ldots\ldots \frac{F_{CLK}}{2} = 0 \ldots .25\ MHz$$

- The frequency code is calculated according the following relation [9]:

$$Code\ F = L = \frac{F.2^{\mathrm{n}}}{F_{CLK}} \qquad (8)$$

So to synthesize three input signals of frequencies $f_{inp1} = 50$ KHz , $f_{inp2} = 100$ KHz , finp3=102 KHz , and fsam= 2 MHz, the frequency code of each one will be:

$$Code\ f_{sam} = L_{SAM} = \frac{f.2^{\mathrm{n}}}{F_{CLK}} = \frac{2X\ 2^{24}}{50} = 671089$$

$$Code\ f_{inp1} = L_{inp1} = \frac{f_{inp1}.\,2^{n}}{f_{sam}} = \frac{0.05X\ 2^{24}}{2} = 414930$$

$$Code\ f_{inp2} = L_{inp2} = \frac{f_{inp2}.\,2^{n}}{f_{sam}} = \frac{0.1X\ 2^{24}}{2} = 838861$$

$$Code\ f_{inp3} = L_{inp3} = \frac{f_{inp3}.\,2^{n}}{f_{sam}} = \frac{0.102X\ 2^{24}}{2} = 855638$$

The block diagram of the digital LPF designed in (Quartus II9.1) environment is shown in figure (5).

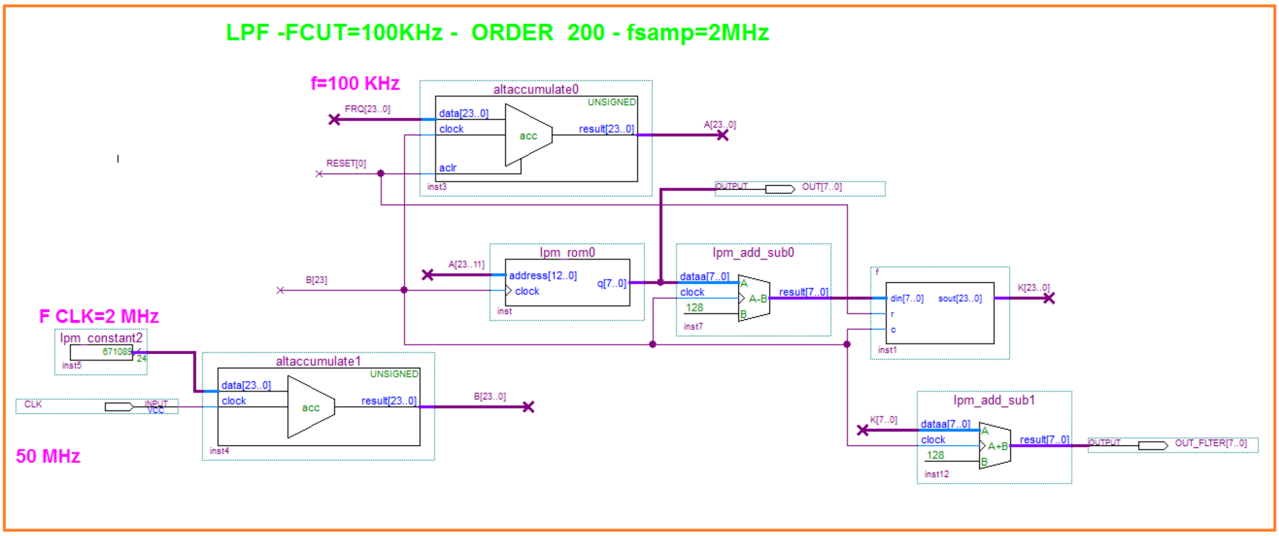


Fig (5) : The block diagram of a digital LPF in (Quartus II9.1)

VII. RESULTS OF DESIGN

The results of the practical design of the digital LPF for different cases (finp1=50 KHz, finp2=100 KHz) in time domain are shown in figure. (6). The results of the practical design of the digital LPF for the same previous cases in frequency domain are shown in figure (7), figure (8), and figure (9). These figures are taken from the screen of digital oscilloscope, and digital spectrum analyzer. We notice from these figures the identification between the theoretical results and the practical results, which indicate the high accuracy of digital synthesizing and filtering operations.

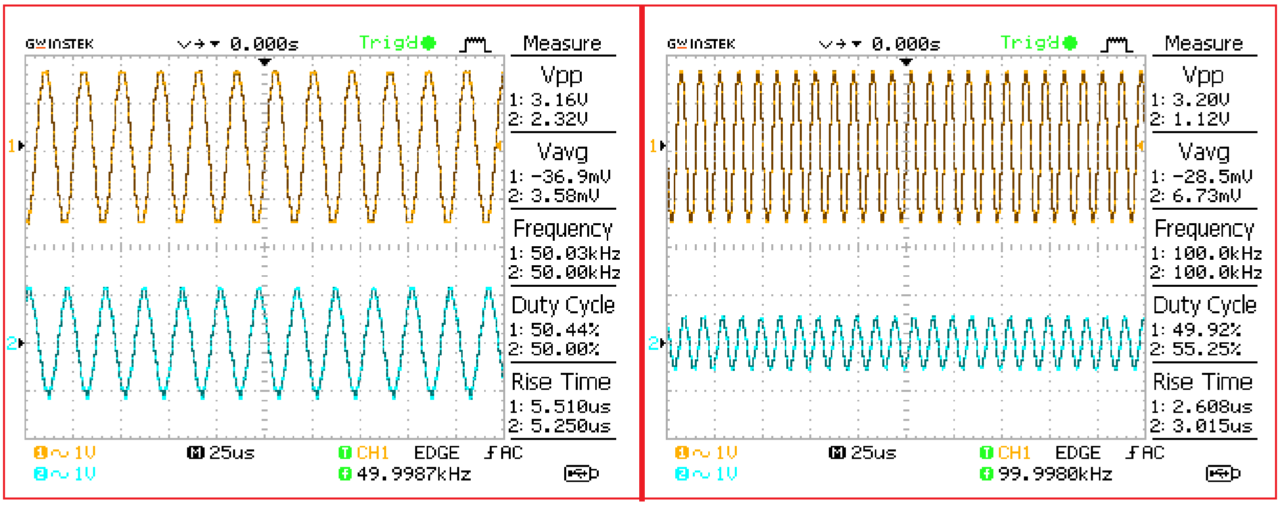


Fig. (6): The output signals for finp1=50KHz, and finp2 =100KHz in time domain.

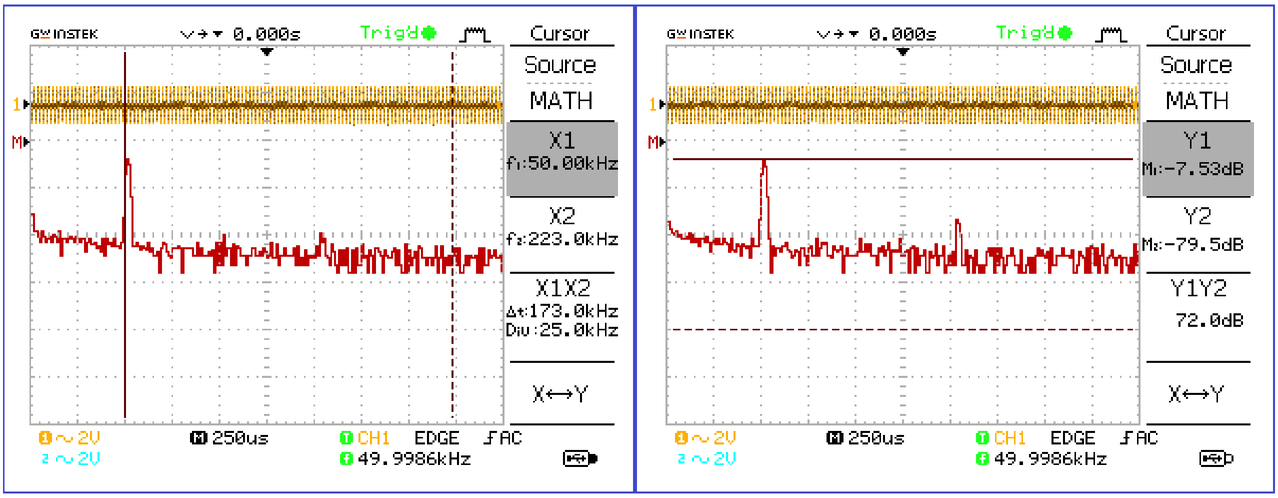


Fig. (7): The output signals for finp1=50KHz in frequency domain.

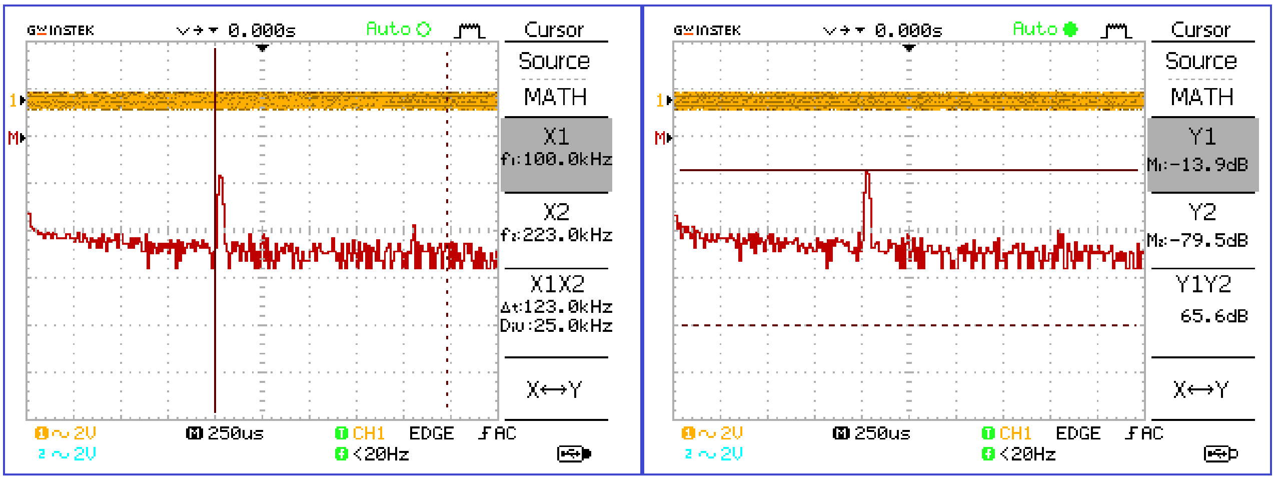


Fig. (8): The output signals for finp2=100KHz in frequency domain

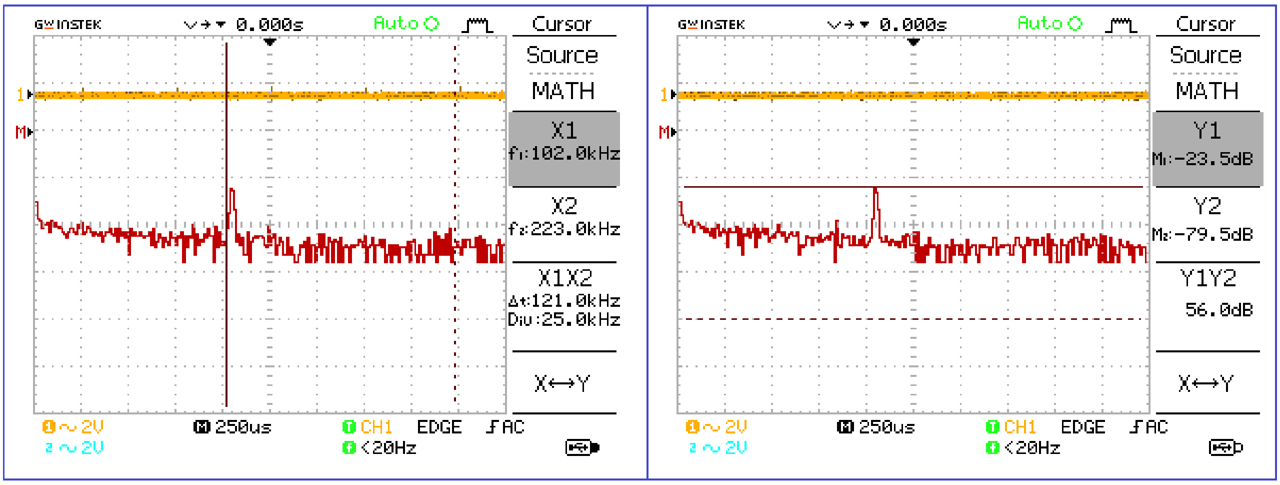


Fig. (9): The output signals for finp3=102KHz in frequency domain

The values [Uout] for different input frequencies are recorded in table (2).

Table (2).			
Values [Uout] For Deference Frequency			
f inp[KHZ]	50	100	102
Uout [dB]	-7.5	-13.9	-23.5
Uout$\{\boldsymbol{FOR}$ f $= \mathbf{102}\} -$ Uout$\{\boldsymbol{FOR}$ f $= \mathbf{50}\} =\mathbf{-23.5} - (\mathbf{-7.5})$ = - 16 dB			

From the figures we notice that the designed LPF works correctly (passes the signal of frequency 50 KHz, and suppresses the signal of frequency 102KHz).

VIII. DISCUSSION AND CONCLUSIONS

-Using digital filtering techniques in communication domain allows implementing different filters (LPF, HPF, PBF, SBF etc) with high accuracy and speed, and with the ability of changing parameters of signals in wide range.

-Using DDFS techniques in communication domain allows implementing the digital processing in the communication receiver on high intermediate frequency.

-We note from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital filtering for signals.

-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).

-The most important thing in this paper is the possibility of changing the frequency of the input signals.
-The performance or specifications of a digital filter can be improved by:

- Increasing the filter order.
- Increasing the number of bits of the input signal.
- Changing the window type.

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BIOGRAPHY

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Dr. Maarouf Yousef: Holds a PhD in electrical engineering in 2001 from the Egypt, technical engineering faculty. Holds assistant professor degree in 2009 from Aleppo university.

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