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Design and Implementation of a Digital Amplitude Demodulator using FPGA

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Abstract: In this paper, we propose the design and implementation mechanism for a digital amplitude demodulator based on the use of Direct Digital Frequency Synthesizer (DDFS) and digital filter using Cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1. The proposed demodulator has the following parameters**:**
-Clock frequency: F_{CLK}=50MHz.
-Sampling frequency: fsam= 40 KHz : (fsam= F_{CLK}/ K=50000 KHz /1250 =40 KHz).
-Cut- off frequency of the low pass filter (LPF): fcut=2 KHz
-Modulation type of signal is: AM, LSB with carrier, USB with carrier.
-The modulating signal is sinusoidal of frequency: fmod=1 KHz , fmod=1.5 KHz (fmod<= fcut).
-Carrier type: is sinusoidal with frequency: fcar=10 KHz.
-The ROM capacity for the stored signal samples 8192X8 bits, and their values are positive within the range from 0 to 255.
-Frequency range: (3 Hz…25 MHz).
-Frequency Resolution: (3 Hz).
-Signal amplitude (5V).
-Digital designs allow the slides to modify and design development for results and better!!! through reprogramming, depending on the user's desire.

Keywords: digital amplitude demodulator ,USB , LSB , DDFS , FPGA.

I. INTRODUCTION

1- The single side band (SSB) signal for upper side band (USB) is given according to the following mathematical relation [1]:

$$V(t)_{usb} = \frac{mV_{car}}{2} cos(w_{car} + w_{mod})t \quad (1)$$

Where:
m: index modulation (m=0,…,1) , $w_{car}=2\pi f_{car}$, $w_{mod}=2\pi f_{mod}$, V_{car} carrier amplitude.
The carrier signal is given according to the following mathematical relation:

$$V(t)_{car} = V_{car} cos w_{car} t \quad (2)$$

The signal of the product carrier and upper side band is given according to the following mathematical relation:

$$V(t)_{usb}\, V(t)_{car} = \left\{\frac{mV_{car}}{2} cos(w_{car} + w_{mod})t\right\} * \{V_{car} cos w_{car} t\} \quad (3)$$

$$V(t)_{usb}\, V(t)_{car} = \frac{m.{V_{car}}^2}{2} cos(w_{car} + w_{mod})t * cos w_{car} t \quad (4)$$

$$V(t)_{usb}\, V(t)_{car} = \frac{m.{V_{car}}^2}{4} \{cos(2w_{car} + w_{mod})t + cos w_{mod} t\} \quad (5)$$

Using the digital LPF with a cut-off frequency (fcut) , the following signal can be removed:

$$\frac{m.{V_{car}}^2}{4} \{cos(2w_{car} + w_{mod})t\} \quad (6)$$

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The output signal of the digital low pass filter (LPF):

$$V(t)_{dem} = \frac{m.V_{car}{}^2}{4} cosw_{mod}t \qquad (7)$$

2- The single side band (SSB) signal for lower side band (LSB) is given according to the following mathematical relation:

$$V(t)_{lsb} = \frac{mV_{car}}{2} cos(w_{car} - w_{mod})t \qquad (8)$$

The carrier signal is given according to the following mathematical relation:

$$V(t)_{car} = V_{car} cosw_{car}t$$

The signal of the product carrier and lower side band is given according to the following mathematical relation :

$$V(t)_{lsb}\, V(t)_{car} = \left\{\frac{mV_{car}}{2} cos(w_{car} - w_{mod})t\right\} * \{V_{car} cosw_{car}t\} \qquad (9)$$

$$V(t)_{lsb}\, V(t)_{car} = \frac{m.V_{car}{}^2}{2} cos(w_{car} - w_{mod})t * cosw_{car}t \qquad (10)$$

$$V(t)_{lsb}\, V(t)_{car} = \frac{m.V_{car}{}^2}{4} \{cos(2w_{car} - w_{mod})t + cosw_{mod}t\} \qquad (11)$$

Using the digital LPF with a cut- off frequency (fcut), the following signal can be removed:

$$\frac{m.V_{car}{}^2}{4} \{cos(2w_{car} - w_{mod})t\} \qquad (12)$$

The output signal of the digital low pass filter (LPF):

$$V(t)_{dem} = \frac{m.V_{car}{}^2}{4} cosw_{mod}t \qquad (13)$$

3- The AM signal (carrier and USB and LSB) is given according to the following mathematical relation:

$$V(t)_{AM} = V_{car} \cos w_{car}t + \frac{mV_{car}}{2} cos(w_{car} + w_{mod})t + \frac{mV_{car}}{2} cos(w_{car} - w_{mod})t \qquad (14)$$

The carrier signal is given according to the following mathematical relation :

$$V(t)_{car} = V_{car} cosw_{car}t$$

The signal of the product carrier and AM signal is given according to the following mathematical relation :

$$V(t)_{AM}\, V(t)_{car} = \left\{V_{car} \cos w_{car}t + \frac{mV_{car}}{2} cos(w_{car} + w_{mod})t + \frac{mV_{car}}{2} cos(w_{car} - w_{mod})t\right\} * \{V_{car} cosw_{car}t\} \qquad (15)$$

$$V(t)_{AM}\, V(t)_{car} = V_{car}{}^2 \cos^2 w_{car}t + \frac{m.V_{car}{}^2}{4} \{cos(2w_{car} + w_{mod})t + cosw_{mod}t\} + \frac{m.V_{car}{}^2}{4} \{cos(2w_{car} - w_{mod})t + cosw_{mod}t\} \qquad (16)$$

Using the digital LPF with a cut off frequency (fcut), the following two signals can be eliminated

$$\frac{m.V_{car}{}^2}{4} \{cos(2w_{car} + w_{mod})t\} + \frac{m.V_{car}{}^2}{4} \{cos(2w_{car} - w_{mod})t\} \qquad (17)$$

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The output signal of the digital low pass filter (LPF) :

$$V(t)_{dem} = \frac{m.V_{car}{}^2}{2} cosw_{mod}t \qquad (18)$$

The block diagram of the digital amplitude demodulator using DDFS and digital filter is shown in the figure (1).

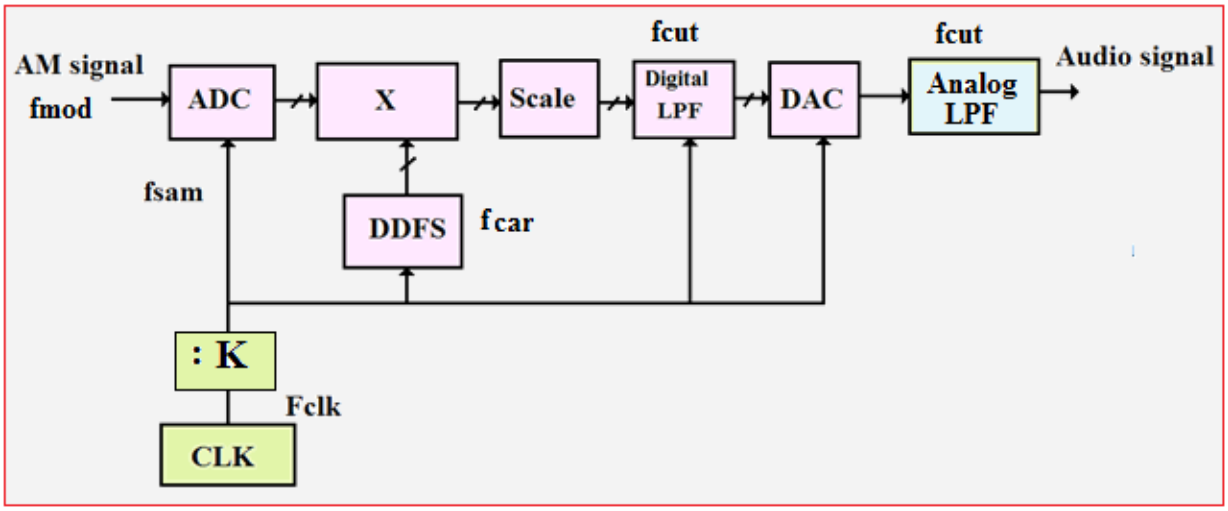

Fig. 1: The block diagram of the digital amplitude demodulator using the DDFS and a digital filter

Reference [2] presents the simple method of design and implementation of a digital amplitude demodulator where the order of the FIR filter order is low which makes the filter frequency response function of lower specification.

II. RESERCH IMPORTANCE AND ITS OBJECTIVES

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-In this paper, a digital amplitude demodulator was designed,implemented and tested based on the use of Digital Direct Frequency Synthesizer (DDFS) using FPGA, VHDL and Graphical programming language with Quartus II 9.1 design environment.

-Using the digital DDFS with mathematical operations (adding , multiply , division ,filtering) , makes the digital demodulation design process flexible, accurate and highly efficient.

-Changing the parameters of modulating signal (frequency and amplitude), carrier frequency explains the difference between digital demodulation and analog demodulation.

III. RESERCH MATERIALS AND ITS WAYS

To design, and test the digital demodulator for different modulation types of signals, the following tools and software are used:

-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].

-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.

-VHDL programming language with Quartus II 9.1 design environment [4].

-Design Environment MATLAB R2008a

-GDS-1052 digital oscilloscope with Free Wave program to take the results.

-PC computer for designing and injecting the design in the FPGA chip.

The block diagram of the laboratory experiment platform [5] is shown in figure (2).

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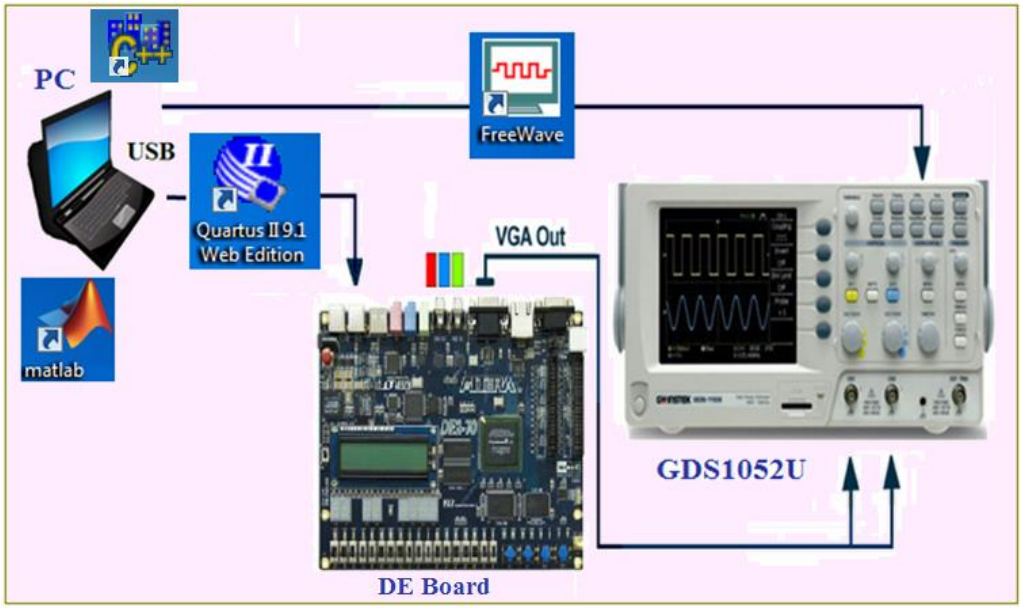

Fig (2): Block diagram of the laboratory experiment platform

IV. THE DESIGN STAGES OF THE DIGITAL AMPLITUDE DEMODULATOR WITH USB USING THE DDFS

1-Convert the analog AM signal to digital signal using ADC for carrier , LSB , USB and AM signals, where : fsam>=2 (fcar+ fmod)

For samples of USB signal :

$$V_{AM}(T_{sam}.n) = \frac{mV_c}{2}\ cos\frac{2\pi.n(f_c + f_m)}{f_{sam}} \qquad (19)$$

2-Formation the samples of a carrier signal using DDFS according to the mathematical relationship.

$$V_{car}(T_{sam}.n) = V_{car}\ cos\ (2\pi f_{car} n\, T_{sam}) = V_{car} cos\frac{2\pi\ f_{car}\ n}{f_{sam}} \qquad (20)$$

3-Formation of the product signal between samples of USB signal and carrier signal samples using DDFS.

$$V_{AM}(T_{sam}.n).V_{car}(T_{sam}.n) =$$

$$= \left\{\frac{mV_{car}}{2}\ cos\frac{2\pi.n(f_{car} + f_{mod})}{f_{sam}}\right\}.\ \left\{V_{car} cos\frac{2\pi\ f_{car}\ n}{f_{sam}}\right\} \qquad (21)$$

$$V_{AM}(T_{sam}.n).V_{car}(T_{sam}.n) = \frac{m\ {V_{car}}^2}{4} cos\{2\pi(2f_{car} + f_{mod})n.T_{sam}\} + \frac{m\ {V_{car}}^2}{4}\cos\ (2\pi.f_{mod}.n.T_{sam})$$

The following component are removed using a digital low pass filter (LPF):

$$\frac{m\ {V_{car}}^2}{4} cos\{2\pi(2f_{car} + f_{mod})n.T_{sam}\} \qquad (22)$$

The output signal of the low pass filter (LPF):

$$V(n)_{dem} = \frac{m\ {V_{car}}^2}{4}\cos(2\pi.f_{mod}.n.T_{sam}) \qquad (23)$$

4- Design the digital low pass filter (LPF) using MATLB and VHDL with the following parameters :
-Type of filter : LPF .
- Filter structure : Direct form - FIR
-Filter order : 199.
-Filter length : 200.
-Sampling frequency : 40 KHz.

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-Frequency of modulating signal : 1 KHz.
-Cut-off frequency of LPF: 2 KHz.
-Window type : Hamming.
-Word length : 8 bits.
The specifications and the magnitude response of a digital filter designed in MATLAB [6] are shown in figure (3).

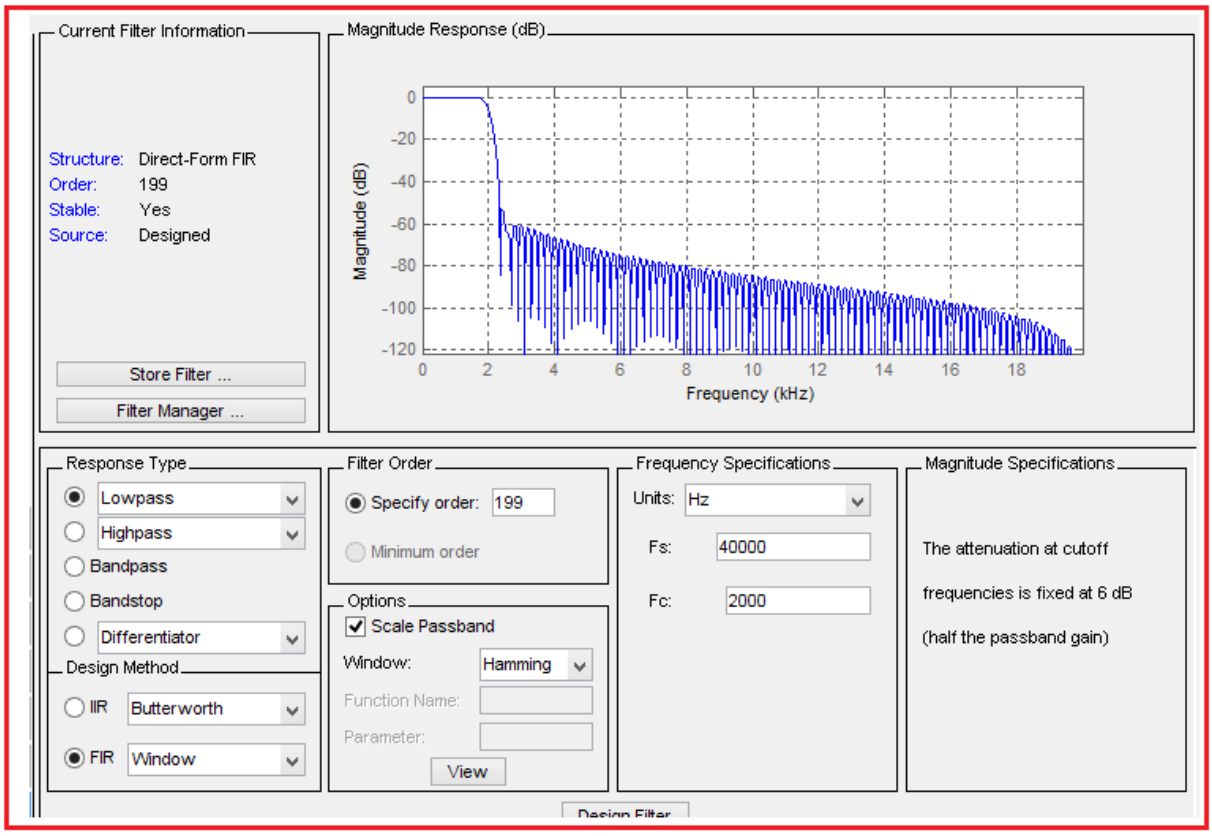

Fig (3): The specifications and the magnitude response of a digital filter designed in MATLAB

V. DESIGN OF THE DIGITAL AMPLITUDE DEMODULATOR USIGN DDFS IN QUARTUS II 9.1

We have a DDFS which has the following parameters:
-The frequency step is : $\delta f = 3\ Hz\ , F_{CLK} = 50\ MHz$.
-The modulating signal (MOD) is sinusoidal of frequency fmod=1 KHz and frequency of carrier signal fcar=10KHz.
-Modulation type: AM, USB, LSB.
-The ROM capacity for the stored signal samples 8192X8 bits and their values are positive within the range from 0 to 255.
-The number of the accumulator bits is computed from the following mathematical relation [7]:

$$\delta f = \frac{F_{CLK}}{2^n} \qquad (24)$$

$$\delta f = \frac{F_{CLK}}{2^n} \Longrightarrow 2^n = \frac{F_{CLK}}{\delta f} = \frac{50\ X\ 10^6}{3} = 24 \text{ bits}$$

-The frequency range for the carrier and modulating signals synthesizer is computed from the following mathematical relation [8]:

$$\Delta f = 0 \ldots . \frac{F_{CLK}}{2} = 0 \ldots .25\ MHz$$

-To synthesize two signals of frequencies $f_{car} = 10$ KHz , $f_{mod} = 1$KHz , the frequency code must be [8]:

$$Code\ F = L = \frac{F.2^n}{F_{CLK}} \qquad (25)$$

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$$Code\ f_{car} = L_{car} = \frac{f_{car}.2^{n}}{F_{CLK}} = \frac{0.01 \text{ x } 2^{24}}{50} = 3355$$

$$Code\ f_{mod} = L_{mod} = \frac{f_{mod}.2^{n}}{F_{CLK}} = \frac{0.001 \text{ x } 2^{24}}{50} = 355$$

The block diagram of a digital amplitude (USB) demodulator is shown in figure (4) [8].

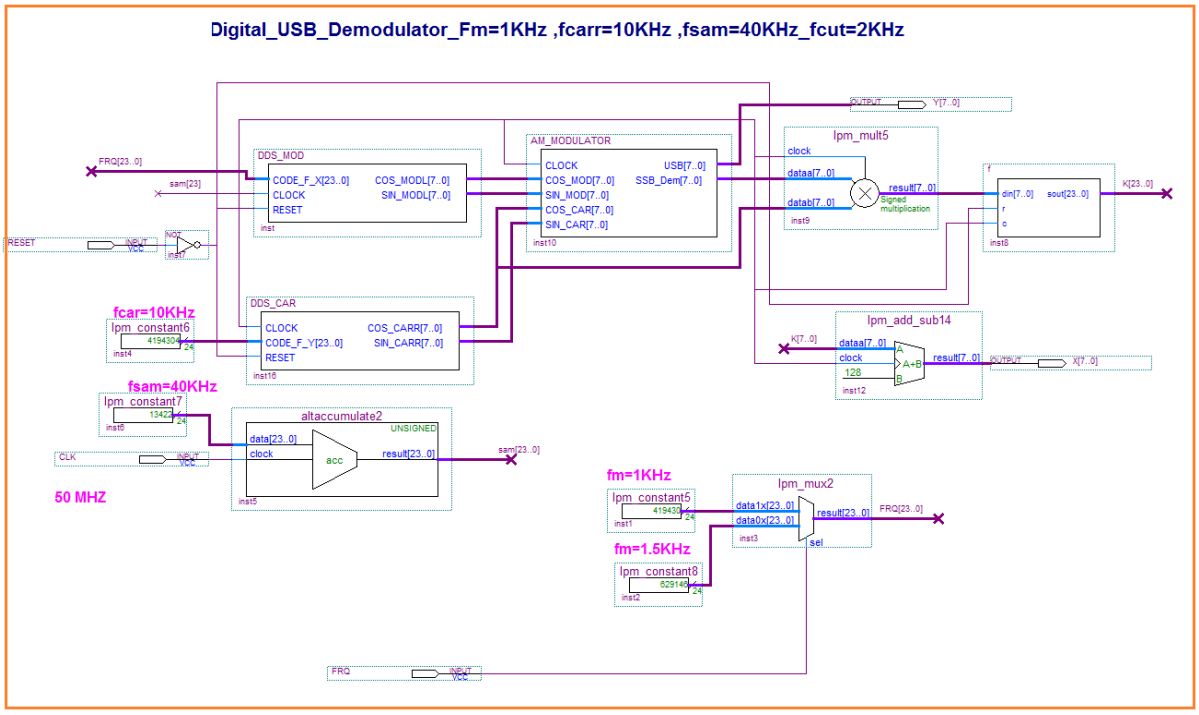

Fig (4) : The block diagram of a digital amplitude (USB) demodulator

VI. RESULTS OF DESIGN

The results of the practical design for the digital amplitude demodulator for different cases (LSB with carrier and USB with carrier) for fmod=1 KHz , fmod=1.5 KHz and fcar =10KHz in time domain according to the previous application using the FPGA chip placed on education and development board DE1 are shown in figure. (5). The results of the practical design for the digital amplitude demodulator for different cases (USB, LSB) in frequency domain according to the previous application using the FPGA chip placed on education and development board DE1 are shown in figure (6) and figure (7). these figures are taken from the screen of digital oscilloscope, and digital spectrum analyzer. We can notice the identification between the theoretical results and the practical results, which indicate the high accuracy of digital synthesizing and modulation operations for these signals. There is a need to refer that the compressing algorithms to a half are used for DDS_MOD, DDS_CAR because of using four DDFS and this requires four ROM memories, these memories exist on the FPGA chip placed on education and development board DE1 of capacity 239616 bits (30 KB).

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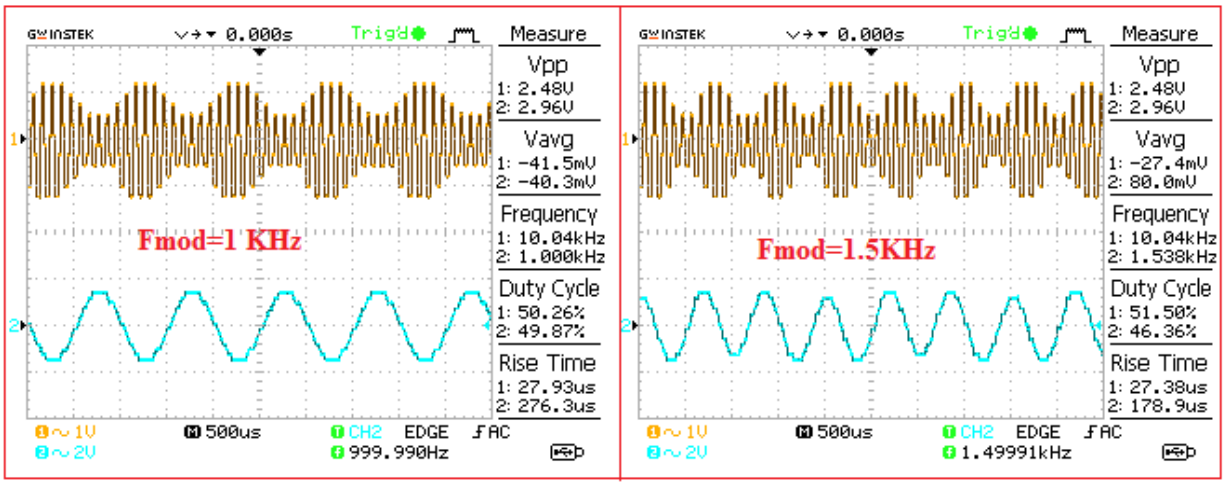

Fig. 5: The AM signal for fmod=1KHz and fmod =1.5KHz in time domain.

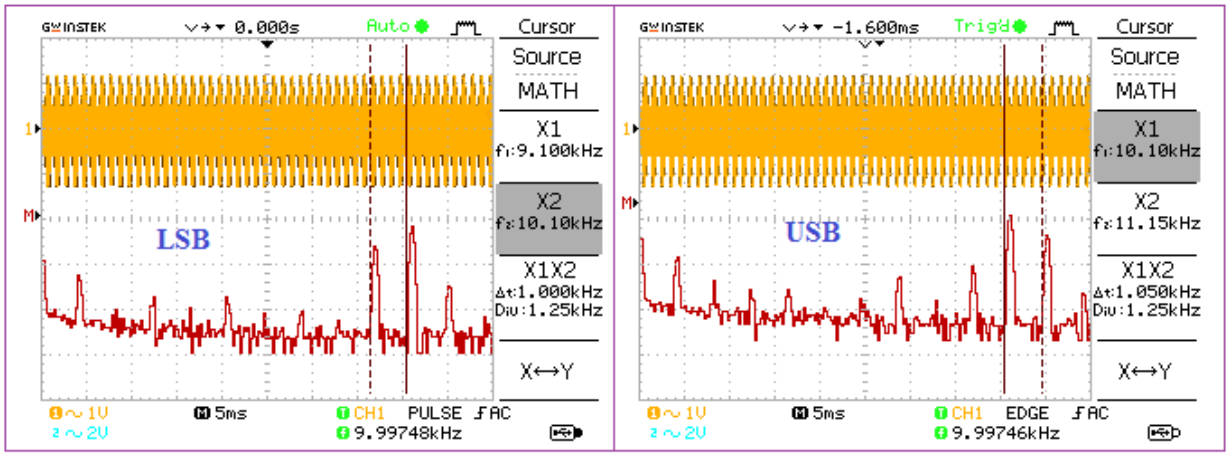

Fig. 6: The AM signal for fmod =1KHz, LSB with carrier and USB with carrier in frequency domain

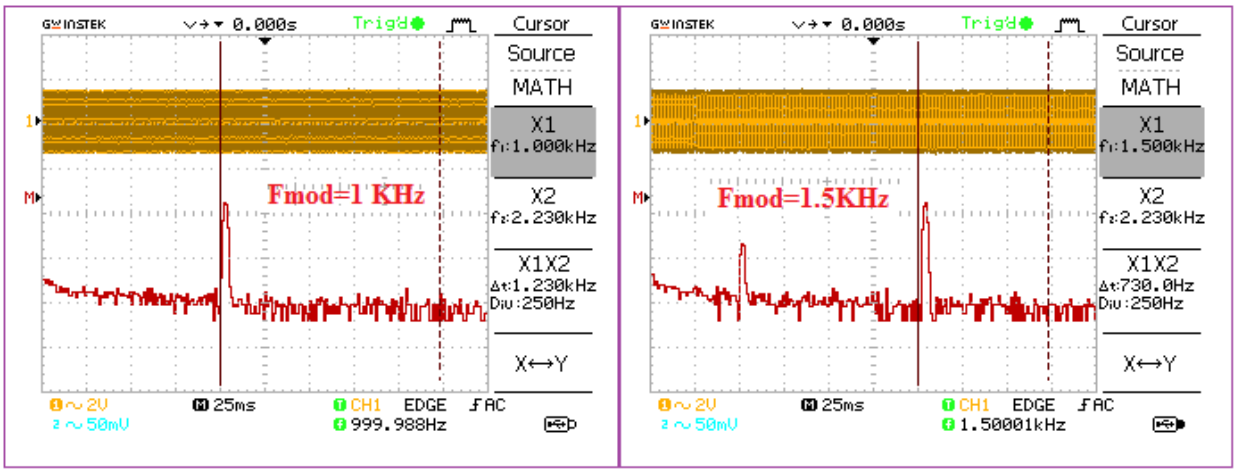

Fig. 7: The modulating signal at the output of digital amplitude demodulator for fmod =1 KHz , and fmod =1.5KHz in frequency domain

VII. DISCUSSION AND CONCLUSIONS

-The use of high-order of FIR filters makes the digital filtering process of the demodulator accurate and efficient.
-The higher order of FIR , the more unwanted frequency components are removed, thus improving the demodulation process.

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-Using DDFS techniques in communication domain allows implementing different digital modulation and demodulation operations (AM, FM, PM, SSB etc) with high accuracy and speed in digital signal synthesizing, and with the ability of changing parameters in wide range.
-Using DDFS techniques in communication domain allows implementing the digital processing in the communication receiver on high intermediate frequency.
-We notice from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital synthesizing and modulation operations for signals.
-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).
-The most important thing in this paper is the possibility of changing the frequency of the modulation signal, and the frequency of the carrier signal.

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BIOGRAPHY

Dr. Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR , university of communication in Leningrad , holds a degree assistant professor in 2009 from Aleppo university.
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Working in the field of programming FPGA by using VHDL, and design of Digital Filters.