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Design and Implementation of a Digital Single Side Band (SSB) Modulator using FPGA

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Abstract
In this paper, we propose the design and implementation mechanism for a digital amplitude single side band modulator based on the use of Direct Digital Frequency Synthesizer (DDFS) using Cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1 . The proposed modulator has the following parameters**:**
-Clock frequency : F_{CLK}=50MHz .
-Modulation type of signal is : Single Side Band (SSB) LSB or USB , Double Side Band (DSB) LSB and USB .
-The modulating signal is sinusoidal of frequency 10 KHz.
-Carrier type: is sinusoidal with frequency 100 KHz .
-The ROM capacity for the stored signal samples 8192X8 bits, and their values are positive within the range from 0 to 255.
-Frequency range : (3 Hz…10 MHz) .
-Frequency Resolution : (3 Hz) .
- Signal amplitude (5V) .
- Digital designs allow the slides to modify and design development for results and better through reprogramming, depending on the user's desire.

Keywords: DSB, SSB, USB, LSB, DDFS, FPGA.

I. INTRODUCTION

The single side band (SSB) signal using the phase shift way is given according to the following mathematical relation [1]:

$$\begin{aligned} &S_{SSB}(t) = S_{\text{mod}}(t) * \text{A}_{\text{car}}.\cos(\text{w}_{\text{car}}\text{t} + \varphi_{\text{car}}) \pm \\ &\pm S_{\text{mod}\perp}(t) * \text{A}_{\text{car}}.\sin(\text{w}_{\text{car}}\text{t} + \varphi_{\text{car}}) \Rightarrow \\ &S_{SSB}(t) = \text{A}_{\text{car}}.\cos(\text{w}_{\text{car}}\text{t} + \varphi_{\text{car}}) * \text{A}_{\text{mod}}.\cos(\Omega_{\text{mod}}\text{t} + \varphi_{\text{mod}}) \pm \\ &\pm \text{A}_{\text{car}}.\sin(\text{w}_{\text{car}}\text{t} + \varphi_{\text{car}}) * \text{A}_{\text{mod}}.\sin(\Omega_{\text{mod}}\text{t} + \varphi_{\text{mod}}) \end{aligned} \quad (1)$$

In case of subtracting (-) we obtain the upper side band USB signal:

$$S_{USB}(t) = \frac{A_{car}A_{\text{mod}}}{2}\cos[(\text{w}_{\text{car}} + \Omega_{\text{mod}})t + \varphi_{\text{car}} + \varphi_{\text{mod}}]$$

In case of adding (+) we obtain the low side band LSB signal:

$$S_{LSB}(t) = \frac{A_{car}.A_{\text{mod}}}{2}\cos[(\text{w}_{\text{car}} - \Omega_{\text{mod}})t + \varphi_{\text{car}} - \varphi_{\text{mod}}]$$

$$S_{DSB}(t) = S_{LSB}(t) + S_{USB}(t)$$

Where: $S_{DSB}(t)$ double side band signal (DSB).

$S_{SSB}(t)$ single side band signal (SSB).

$S_{USB}(t)$ upper side band signal (USB).

$S_{LSB}(t)$ lower side band signal (LSB).

$S_{\text{mod}}(t)$ the modulation signal.

$S_{\text{mod}\perp}(t)$ the modulation signal which is orthogonal with $S_{\text{mod}}(t)$ signal.

A_{car} amplitude of carrier signal.

φ_{car} phase of carrier signal.

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A_{mod} amplitude of modulation signal.

φ_{mod} phase of modulation signal.

$$w_{car} = 2\pi F_{car},\ w_{mod} = 2\pi F_{mod}.$$

The block diagram of the SSB amplitude modulator using phase shift way is shown in figure (1), and figure (2) shows the functional diagram of the SSB digital amplitude modulator.

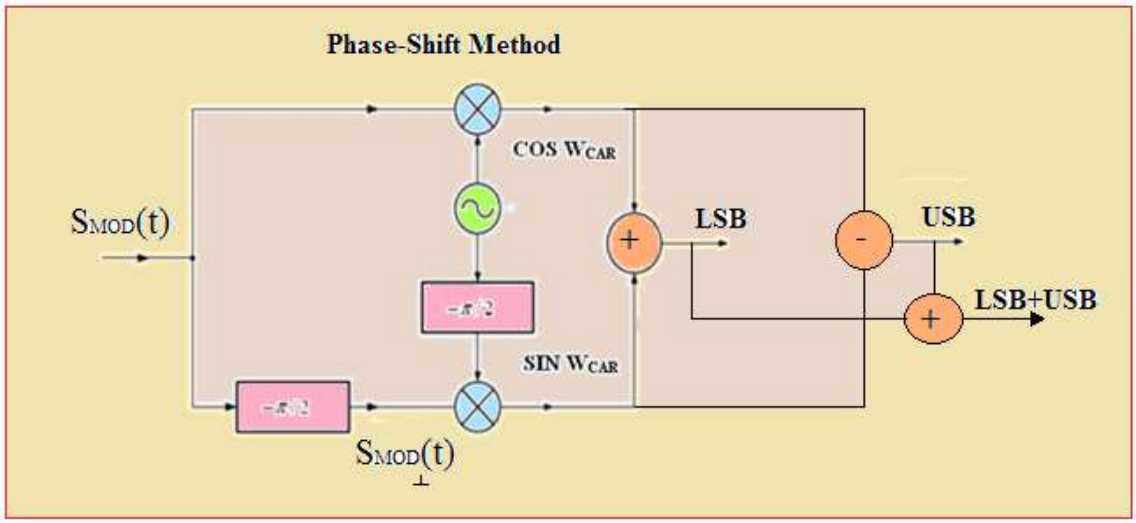

Fig. 1: The block diagram of the SSB amplitude modulator using the phase shift way

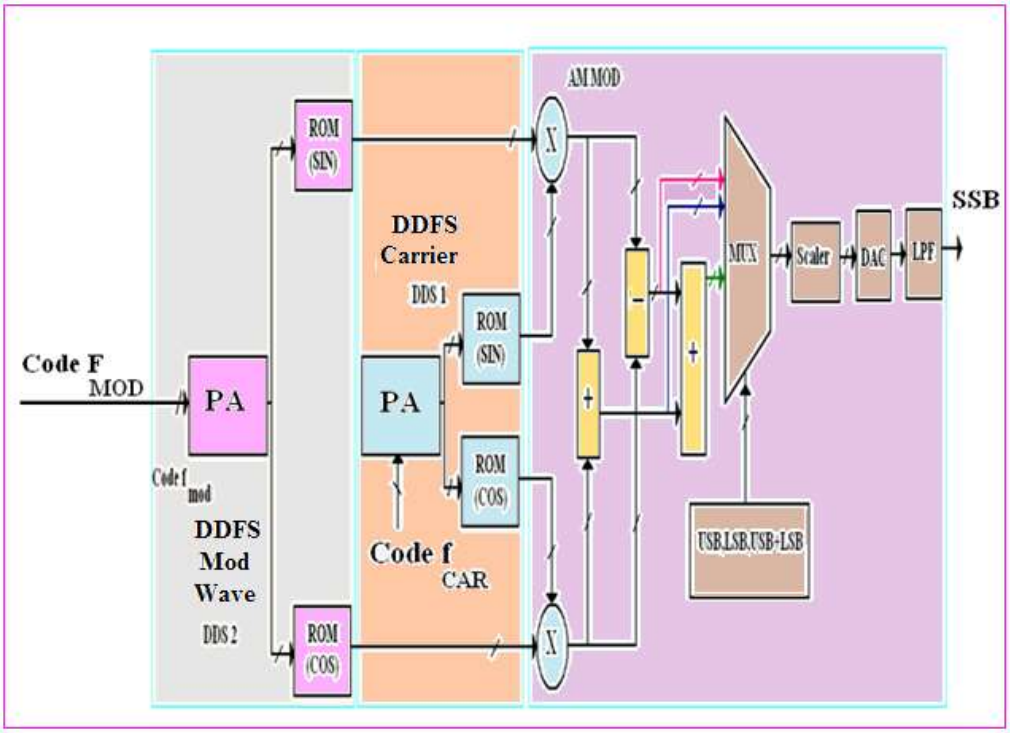

Fig. 2: The functional diagram of the SSB amplitude modulator using the phase shift way

Reference [2] presents the simple method of design and implementation of a digital SSB (LSB or USB) amplitude modulator where the modulation factor and the frequency of the modulation wave are constants.

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II. RESERCH IMPORTANCE AND ITS OBJECTIVE

- In this paper a digital SSB modulator was designed, implemented and tested based on the use of Digital Direct Frequency Synthesizer (DDFS) using FPGA, VHDL and Graphical programming language with Quartus II 9.1 design environment.
- Using the digital DDFS with mathematical operations (adding , multiply , division) makes the digital modulation - design process flexible, accurate and highly efficient.
- Changing the parameters of modulating signal (frequency and amplitude) , carrier frequency explains the difference between digital modulation and analog modulation.

III. RESERCH MATERIALS AND ITS WAYS

To design, and test the digital modulators for different modulation types of signals, the following tools and software are used:
-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].
-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment [4].
-Design Environment MATLAB R2008a
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [5] is shown in figure (3).

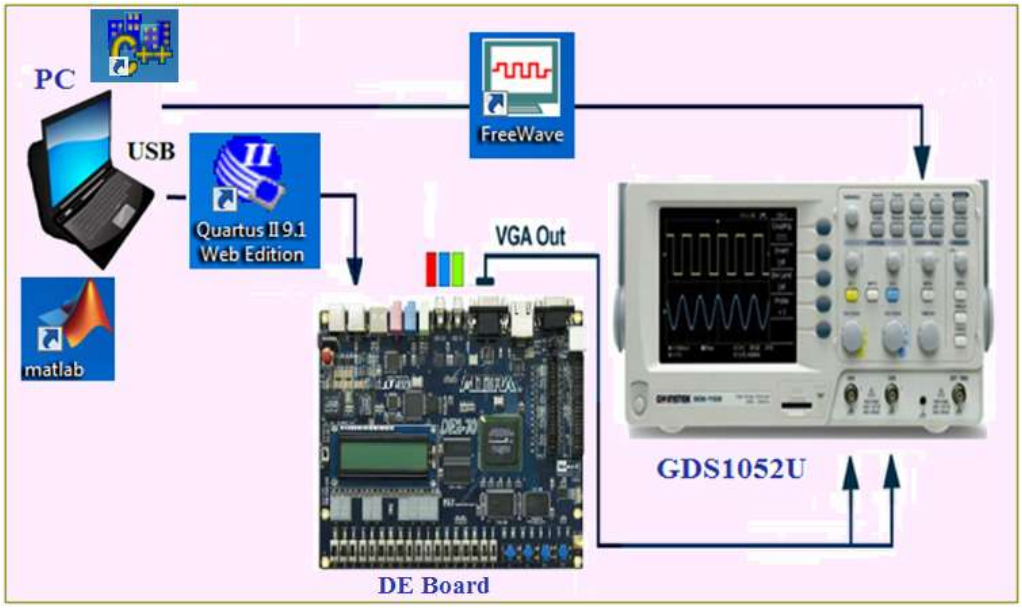

Fig (3) Block diagram of the laboratory experiment platform

IV. THE DESIGN STAGES OF THE DIGITAL SSB MODULATOR USING THE PHASE SHIFT WAY

1-Computing the frequency range of the DDFS.
2-Computing the number of the accumulator bits beginning with the required frequency step.
3-Computing the frequency codes for the carrier signal and modulation signal (Code f_{CAR}, Code F_{MOD}).
4-Computing the parameters of the digital SSB modulator (choose LSB or USB or LSB+USB)
5-Designing the digital SSB modulator circuit using digital chips FPGA within the designing programming environment Quartus II 9.1. [6].

V. DESIGN OF THE DIGITAL SSB MODULATOR USIGN THE PHASE SHIFT WAY

We have a DDFS which has the following parameters:
-The frequency step is $\delta f = 3Hz$, $F_{CLK} = 50MHz$.

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-The modulating signal (MOD) is sinusoidal of frequency Fmod=10 KHz ,and frequency of carrier Fcar=100KHz.
-Modulation type: LSB, USB, LSB+USB.
-The ROM capacity for the stored signal samples 8192X8 bits and their values are positive within the range from 0 to 255.
-The number of the accumulator bits is computed from the following mathematical relation [7]:

$$\delta f = \frac{F_{CLK}}{2^n} \qquad (2)$$

$$\delta f = \frac{F_{CLK}}{2^n} \Rightarrow 2^n = \frac{F_{CLK}}{\delta f} = \frac{50*10^6}{3} \Rightarrow n = 24bit$$

-The frequency range for the carrier and modulating signals synthesizer is computed from the following mathematical relation [8]:

$$\Delta f = 0....\frac{F_{CLK}}{2} = 0...25MHz$$

-To synthesize two signals of frequencies $F_{car} = 100KHz, F_{\mathrm{mod}} = 10KHz$, the frequency code must be [7]:

$$Code\ \mathrm{F} = L = \frac{F.2^n}{F_{CLK}} \qquad (3)$$

$$Code\ \mathrm{F_{car}} = L_{car} = \frac{F_{car}.2^n}{F_{CLK}} = \frac{0.1*2^{24}}{50} = 33554$$

$$Code\ F_{\mathrm{mod}} = \mathrm{L_{mod}} = \frac{F_{\mathrm{mod}}.2^n}{F_{CLK}} = \frac{0.01*2^{24}}{50} = 3355$$

-The modulation type: the modulation type is chosen through passing USB samples or LSB samples or USB+LSB samples through the multiplexer MUX to the scaling algorithm, then the basic mathematical relation of the SSB amplitude modulation is realized in digital form:

$$\begin{aligned} S_{LSB}(i) &= \cos w_{car} i * \cos \Omega_{\mathrm{mod}} i + \sin w_{car} i * \sin w_{\mathrm{mod}} i \\ S_{USB}(i) &= \cos w_{car} i * \cos \Omega_{\mathrm{mod}} i - \sin w_{car} i * \sin w_{\mathrm{mod}} i \\ S_{USB+LSB}(i) &= S_{LSB}(i) + S_{USB}(i) = \\ &= \cos w_{car} i * \cos \Omega_{\mathrm{mod}} i + \sin w_{car} i * \sin w_{\mathrm{mod}} i + \\ &+ \cos w_{car} i * \cos \Omega_{\mathrm{mod}} i - \sin w_{car} i * \sin w_{\mathrm{mod}} i \end{aligned} \qquad (4)$$

Where: (i) the sample number, $S_{car}(i)$ carrier signal samples, $S_{\mathrm{mod}}(i)$ modulation signal samples, $S_{LSB}(i), S_{USB}(i), S_{USB+LSB}(i)$ amplitude signal samples of the SSB (LSB, USB, LSB+USB).

-The SSB amplitude modulation in digital way is considered as multiplication, dividing, and adding operations for digital samples of the modulation signal and carrier signal according to the previous relation so there is need to realize a synchronization for these operations through one clock pulses $F_{CLK} = 50MHz$ for all operations as shown in figure (4) , figure (5), figure (6) , figure (7).

-The results of multiplication, adding, subtracting, and dividing for positive and negative samples are large numbers out of the required words length limits, and sometimes redundancy operations take places for these values causing a big and illogical errors in these operations. So there is need to make a scaling operation where we obtain a values within the required ranges in all digital modulation stages through dividing, multiplication, adding, and subtracting of the operations, and this what realize it the scaling algorithm.
The general functional diagram of the modulator SSB using the programming environment Quartus II 9.1 [8] is shown in figure (4) due to $F_{car} = 100KHz, F_{\mathrm{mod}} = 10\,KHz$ and it consists of:

-The modulation signal synthesizer (DDS_MOD) .
-The carrier signal synthesizer (DDS_CAR) .
-SSB amplitude modulator (SSB_MODULATOR) .
-Clock pulses generator of frequency $F_{CLK} = 50MHz$ for all components of the digital SSB amplitude modulator.
-Scaling algorithm.

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Figure (5) shows the detailed diagram of the modulation signal synthesizer which is considered as a DDFS. Figure (6) shows the detailed diagram of the carrier signal synthesizer. Figure (7) shows the detailed diagram of the SSB amplitude modulator which is considered as a set of multipliers and dividers of the modulation signal and carrier signal samples.

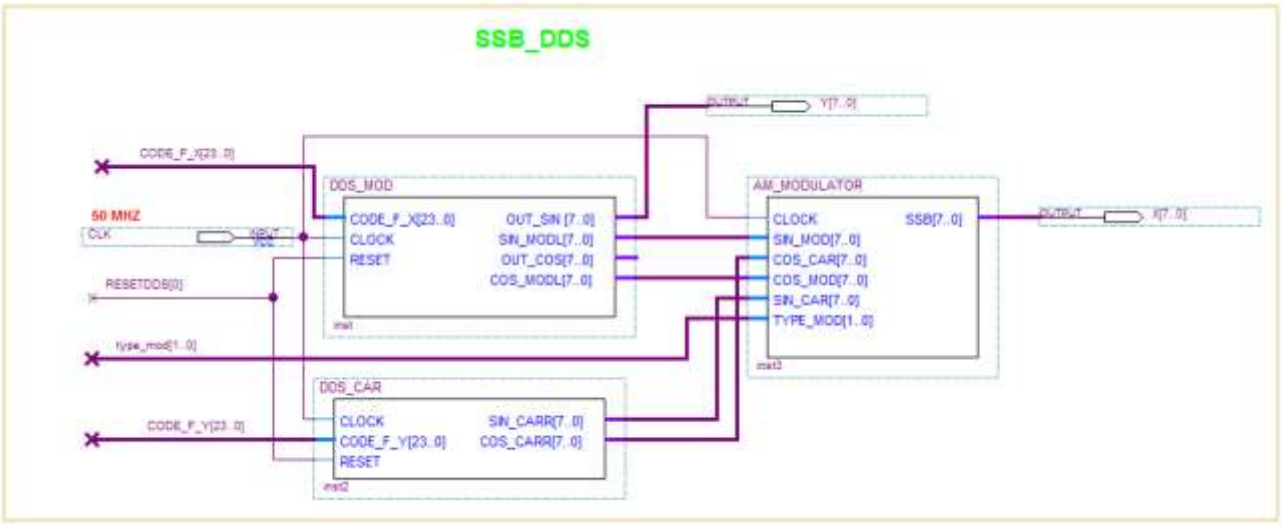

Fig. 4: The general functional diagram of the digital SSB modulator using Quartus II 9.1

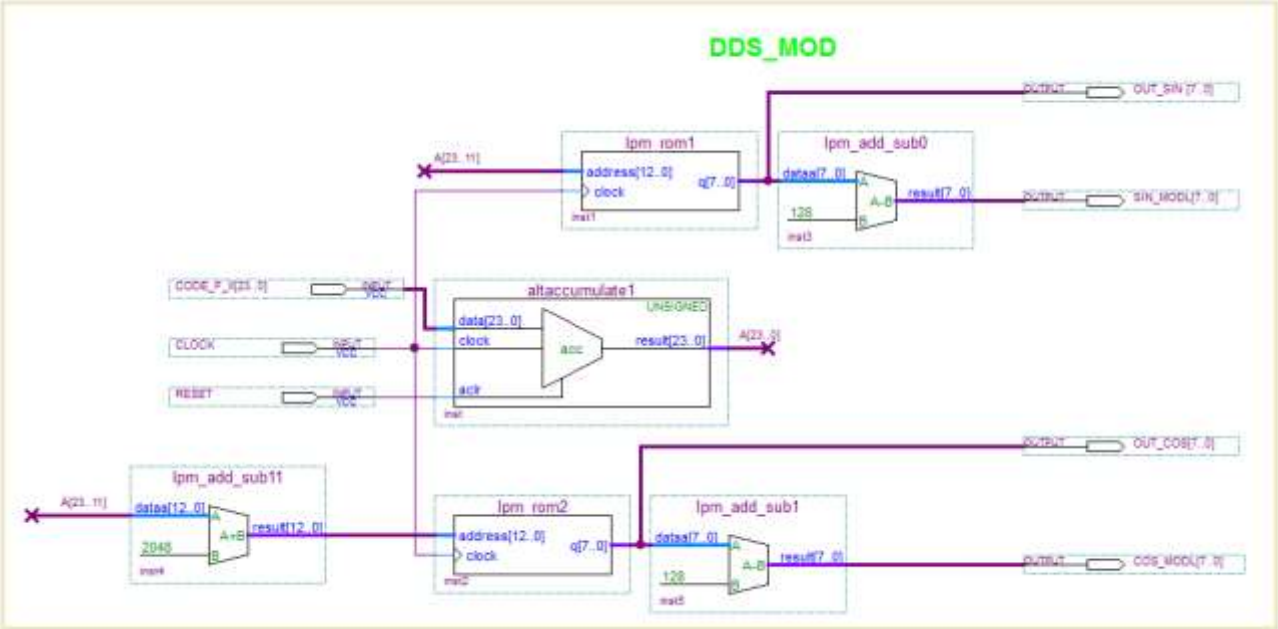

Fig. 5: The detailed diagram of the modulation signal synthesizer using Quartus II 9.1

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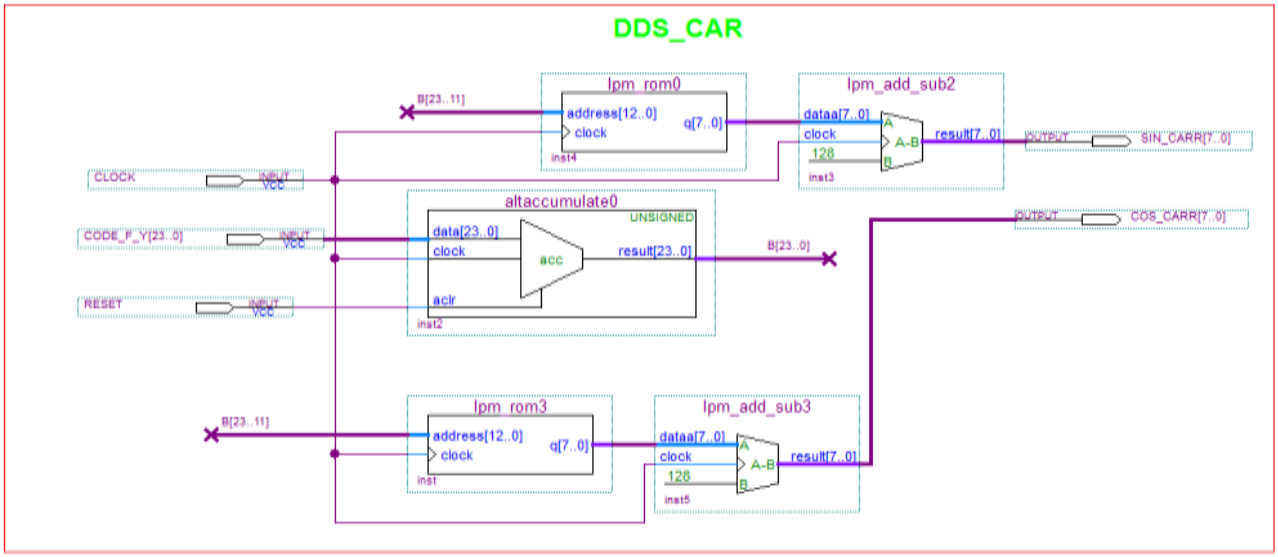

Fig. 6: The detailed diagram of the carrier signal synthesizer using Quartus II 9.1

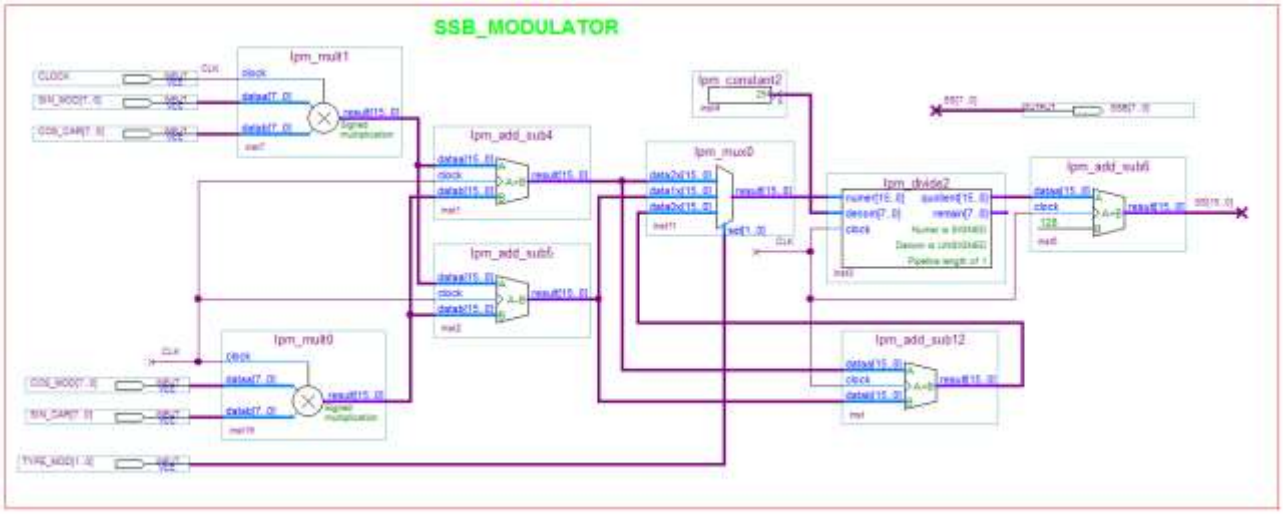

Fig. 7: The detailed diagram of the digital SSB modulator using Quartus II 9.1

VI. RESULTS OF DESIGN

The results of the practical design for the digital SSB modulator for different cases (carrier , modulation and SSB signals) for Fmod=10 KHz and Fcar =100KHz in time domain are shown in figure. (8). The results of the practical design for the digital SSB modulator for different cases (USB, LSB, USB+LSB) in frequency domain are shown in figure (9). These figures are taken from screen of a digital oscilloscope, and a digital spectrum analyzer. We not from the practical results the identification between the theoretical results and the practical results which indicates the high accuracy of digital synthesizing and modulation operations for these signals. There is a need to refer that the compressing algorithms to a half are used for DDS_MOD, DDS_CAR because of using four DDFS and this requires four ROM memories, these memories are existence on the FPGA chip placed on education and development board DE1 of capacity 239616 bits (30 KB).

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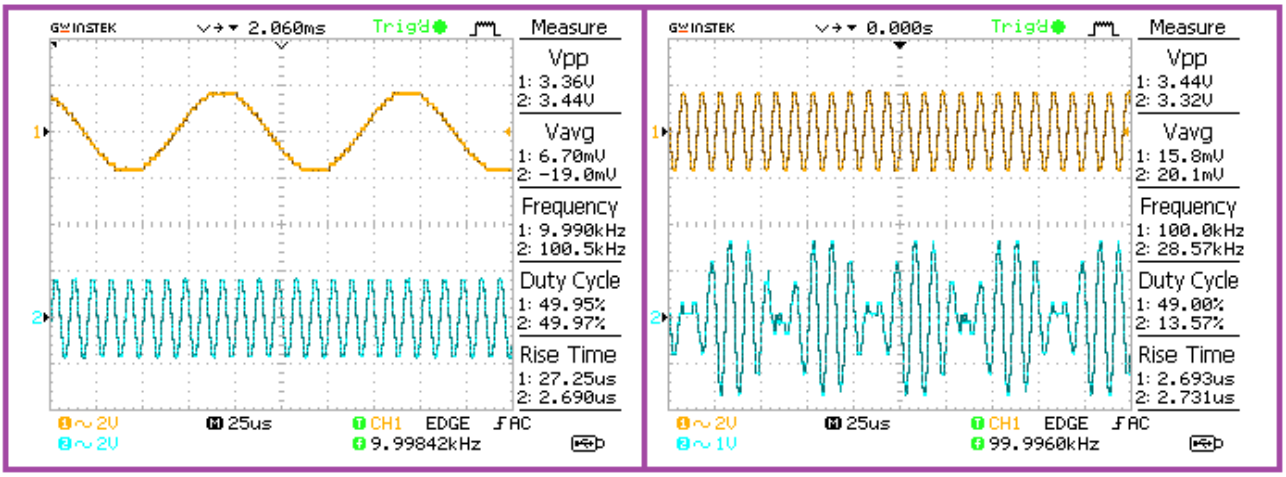

Fig. 8: The practical results of the digital SSB modulator in time domains for modulation ,carrier and DSB signals

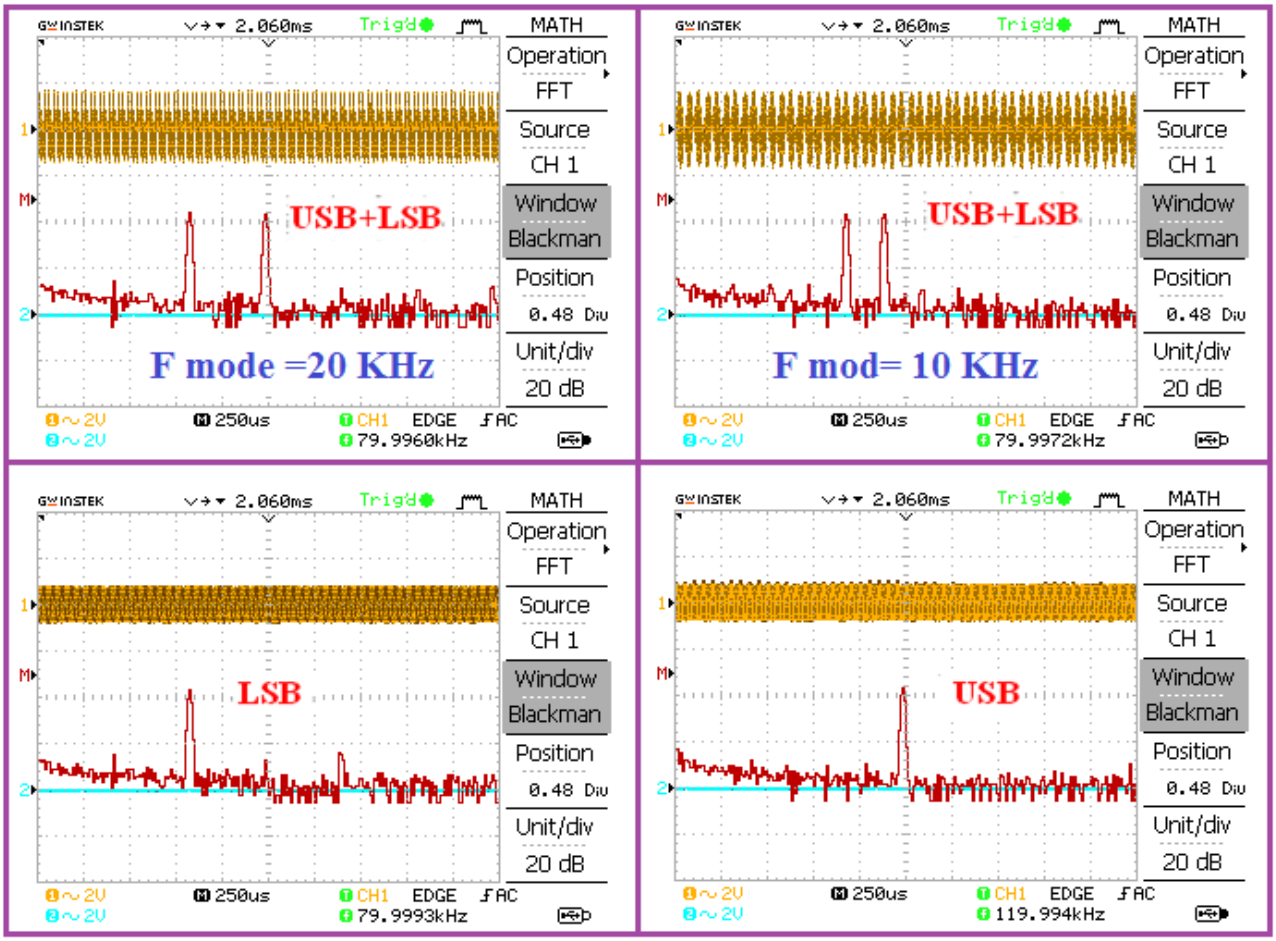

Fig. 9: The practical results of the digital SSB modulator in frequency domains for cases USB, LSB, USB+LSB for Fmod=20 KHz and Fmod=10KHz

VII. DISCUSSION AND CONDLUSION

-Using DDFS techniques in communication domain allows implementing different digital modulation operations (AM, FM, PM, SSB etc) with high accuracy and speed in digital signal synthesizing, and with the ability of changing parameters in wide range.
-Using DDFS techniques in communication domain allows implementing the digital processing in the communication receiver on high intermediate frequency.

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-We note from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital synthesizing and modulation operations for signals.
-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).
-The most important thing in this paper is the possibility of changing the frequency of the modulation signal, and the frequency of the carrier signal.

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BIOGRAPHY

Dr. Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR , university of communication in Leningrad , holds a degree assistant professor in 2009 from Aleppo university.
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Working in the field of programming FPGA by using VHDL, and design of Digital Filters.