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Design And Implementation Of a Digital Amplitude Modulator (AM) using FPGA

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Abstract
In this paper, we propose the design and implementation mechanism for a digital amplitude modulator based on the use of Direct Digital Frequency Synthesizer (DDFS) using Cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1 . The proposed modulator has the following parameters**:**
-Clock frequency : F_{CLK}=50MHz .
-Modulation type of signal is : AM with carrier , AM without carrier.
-The modulating signal is sinusoidal of frequency 10 KHz.
-Modulation factor (m= 0 to 100).
-Carrier type: with carrier, without carrier.
-The ROM capacity for the stored signal samples 8192X8 bits, and their values are positive within the range from 0 to 255.
-Frequency range : (3 Hz…10 MHz) .
-Frequency Resolution : (3 Hz) .
- Signal amplitude (5V) .
- Digital designs allow the slides to modify and design development for results and better through reprogramming, depending on the user's desire.

Keywords: Digital Amplitude Modulator , AM, DDFS , FPGA.

I. INTRODUCTION

The general principle of the digital modulation using DDFS, as we have seen previously, depends on carrying out mathematical operations (adding, multiplying, dividing) between the modulating signal samples (information signal) and the synthesized signal samples (carrier signal), or between the modulating signal samples and the phase accumulating value for the digital frequency synthesizer. For the frequency modulation, the adding operation is carried out between the modulating signal samples and the phase accumulating value at the accumulator input, but for the phase modulation, the adding operation is carried out between the modulating signal samples and the phase accumulating value at the accumulator output. For the amplitude modulation, the multiplying operation is carried out between the carrier signal samples (ROM output) and the modulating signal samples (ADC output). The functional diagram of the frequency, phase, and amplitude modulation operations using DDFS is shown in the figure. 1. The basic mathematical relation of modulation operations (AM, FM, PM) [1] is:

$$S(t) = A(t).A_{CAR}\sin\{[(w_{CAR} + w(t)]t + \varphi(t)\} \qquad (1)$$

Where $A(t)$ the amplitude modulating signal, $w(t)$ the frequency modulating signal, $\varphi(t)$ the phase modulating signal.

Paper [2] presents the simple method of design and implementation of an digital amplitude modulator where the modulation factor and the frequency of the modulation wave are constants.

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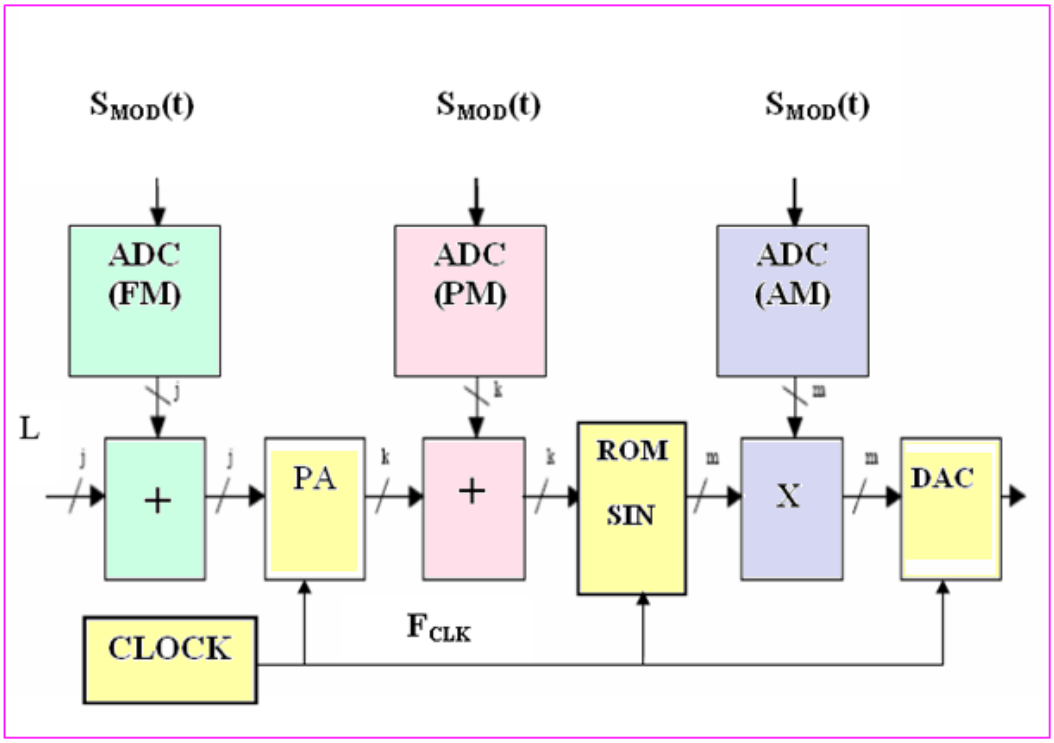

Fig. 1: The functional diagram of frequency, phase, and amplitude modulation operations using DDFS

II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

-In this paper digital AM and SSB modulators were designed, implemented and tested based on the use of Digital - Direct Frequency Synthesizer (DDFS) using FPGA, VHDL and Graphical programming language with Quartus II 9.1 design environment.
-Using the digital DDFS with mathematical operations (adding , multiply , division) , makes the digital modulation - design process flexible, accurate and highly efficient.
-Changing the parameters of modulating signal (frequency and amplitude) , carrier frequency explains the difference between digital modulation and analog modulation.

III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the digital modulators for different modulation types of signals, the following tools and software are used:
-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].
-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment [4].
-Design Environment MATLAB R2008a
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [5] is shown in figure (2).

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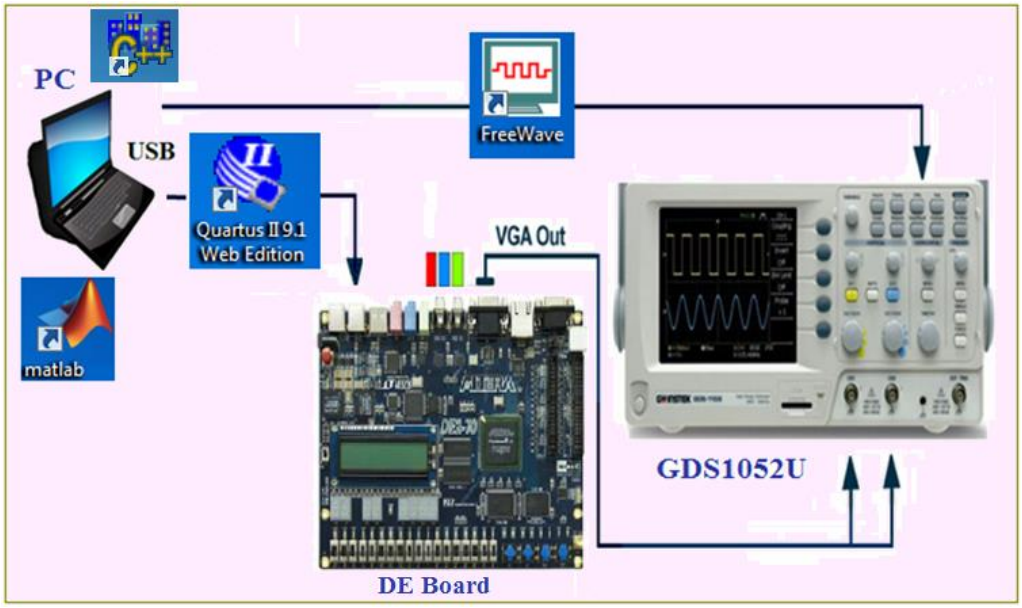

Fig (2) Block diagram of the laboratory experiment platform

IV. THE DIGITAL AM MODULATOR

To perform the AM modulation, a multiplier is placed between the ROM and DAC of the DDFS, the AM is carried out using DDFS according to the block diagram shown in figure. 3, which consists of DDFS to synthesize the carrier signal of frequency W_{CAR} , and amplitude modulator which consists of ADC for the modulating signal samples, and multiplier of the carrier signal and modulating signal samples. The ROM output samples are applied at the first input of the multiplier, and the modulating signal amplitude samples are applied at the second input after transforming them to digital values by ADC where its capacity (number of bits) equals to DAC capacity, by changing the modulating signal amplitude, the ADC code changes, so the amplitude modulation is carried out, the digital synthesizer AD9854 contains a special multiplier for this purpose. figure. 4 shows the functional diagram of the digital AM modulator.

We saw in DDFS topic the possibility of frequency and phase changing of the synthesized signal samples by easy and flexible form. This allows realizing the phase and frequency modulation according to the following mathematical relation:

$$S_{AM}(t) = S_{MOD}(t).S_{CAR}(t) = S_{M0D}(t).\cos[w_{CAR}t + \varphi_{CAR}] \qquad (2)$$

By analyzing the previous relation we note that it is possible to change the synthesized signal amplitude through carrying out multiplication operation for the synthesizer signal samples and modulating signal samples, so this allows synthesizing amplitude modulation signal AM. The number of ROM memory bits (m) must be equals to the ADC bits number for the modulating signal, then the result of multiplication between ROM samples and ADC samples has a bits number of 2m, so we need to place a scaler where the bits number of the scaler output must be equal to the DAC bits number , in this case the scaler is considered as divided by 2.

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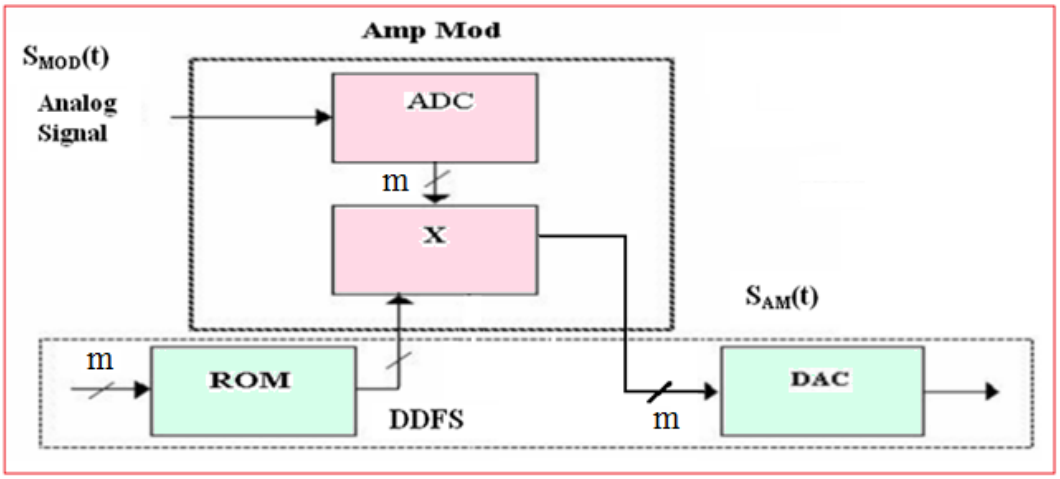

Fig. 3: The block diagram of the digital AM modulator

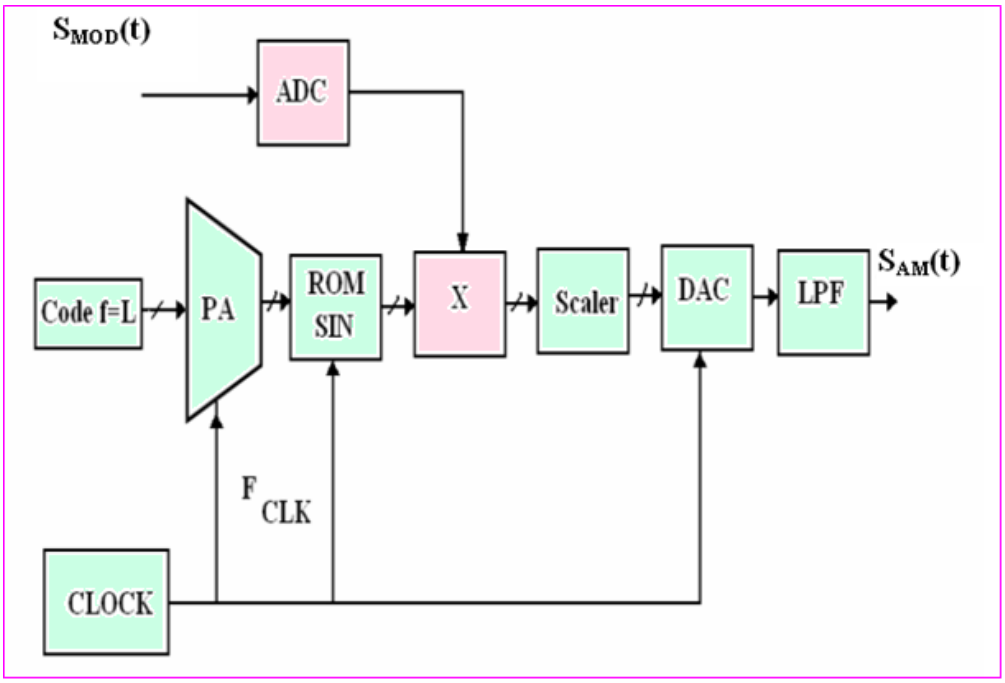

Fig. 4: The functional diagram of the digital AM modulator using DDFS

The AM signal in case of carrier suppression is given according to the following mathematical relation [6]:

$$S_{AM}(t) = A_{CAR}.\cos(w_{CAR}t + \varphi_{CAR}) * A_{MOD}.\cos(\Omega_{MOD}t + \varphi_{MOD})$$

$$S_{AM}(t) = \frac{A_{CAR}.A_{MOD}}{2}\cos(w_{CAR}t + \varphi_{CAR} + \Omega_{MOD}t + \varphi_{MOD}) +$$

$$+ \frac{A_{CAR}.A_{MOD}}{2}\cos(w_{CAR}t + \varphi_{CAR} - \Omega_{MOD}t - \varphi_{MOD}) \quad (3)$$

$$S_{AM}(t) = \frac{A_{CAR}.A_{MOD}}{2}\cos[(w_{CAR} + \Omega_{MOD})t + \varphi_{CAR} + \varphi_{MOD}] +$$

$$+ \frac{A_{CAR}.A_{MOD}}{2}\cos[(w_{CAR} - \Omega_{MOD})t + \varphi_{CAR} - \varphi_{MOD}]$$

While the AM signal in case of carrier existence is given according to the following mathematical relation:

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$$S_{AM}(t) = \mathrm{A_{CAR}}.\cos(\mathrm{w_{CAR}}t + \varphi_{\mathrm{CAR}}) +$$
$$+ \mathrm{A_{MOD}}.\cos(\Omega_{MOD}t + \varphi_{MOD}) * \mathrm{A_{CAR}}.\cos(\mathrm{w_{CAR}}t + \varphi_{\mathrm{CAR}}) \Rightarrow \quad (4)$$
$$S_{AM}(t) = \mathrm{A_{CAR}}.\cos(\mathrm{w_{CAR}}t + \varphi_{\mathrm{CAR}})[1 + \mathrm{m}.\cos(\Omega_{MOD}t + \varphi_{MOD})]$$
$$\mathrm{m} = \mathrm{A_{MOD}}/\mathrm{A_{CAR}}$$
$$S_{AM}(t) = \mathrm{A_{CAR}}.\cos(\mathrm{w_{CAR}}t + \varphi_{\mathrm{CAR}}) +$$
$$+ \frac{\mathrm{A_{CAR}}.\mathrm{m}}{2}\cos(\mathrm{w_{CAR}}t + \varphi_{\mathrm{CAR}} + \Omega_{MOD}t + \varphi_{MOD}) +$$
$$+ \frac{\mathrm{A_{CAR}}.\mathrm{m}}{2}\cos(\mathrm{w_{CAR}}t + \varphi_{\mathrm{CAR}} - \Omega_{MOD}t - \varphi_{MOD}) \Rightarrow$$
$$S_{AM}(t) = \mathrm{A_{CAR}}.\cos(\mathrm{w_{CAR}}t + \varphi_{\mathrm{CAR}}) + \quad (5)$$
$$+ \frac{\mathrm{A_{CAR}}.\mathrm{m}}{2}\cos[(\mathrm{w_{CAR}} + \Omega_{MOD})t + \varphi_{\mathrm{CAR}} + \varphi_{MOD}] +$$
$$+ \frac{\mathrm{A_{CAR}}.\mathrm{m}}{2}\cos[(\mathrm{w_{CAR}} - \Omega_{MOD})t + \varphi_{\mathrm{CAR}} - \varphi_{MOD}]$$

Where:
$A_{CAR}, W_{CAR}, \varphi_{CAR}$: the initial amplitude, frequency, and phase of the carrier signal.
$A_{MOD}, \Omega_{MOD}, \varphi_{MOD}$: the initial amplitude, frequency, and phase of the modulating signal.
$m = 0...1$: modulation factor.
figure. 5 shows the time diagram of the AM signal, which consists of the carrier signal (Carrier Wave) and modulation signal (Modulation Wave) and amplitude modulation signal (AM signal). figure. 6 shows the time diagram of the AM modulator operation due to different values of modulation factor $(m = 0, m = 0.5, m = 1)$. The spectrum of the AM signal in case of carrier suppression consists of two components, the first is of frequency $(W_{CAR} + \Omega_{MOD})$ and the second is of frequency $(W_{CAR} - \Omega_{MOD})$, the spectrum of the AM signal in case of carrier existence consists of three components the first is of frequency (W_{CAR}), the second is of frequency $(W_{CAR} + \Omega_{MOD})$, and the third is of frequency $(W_{CAR} - \Omega_{MOD})$, the amplitude, and phase spectrum for this case is shown in figure.7.
The block diagram of the AM algorithm using DDFS is shown in figure.8. The functional diagram of the AM algorithm using DDFS is shown in figure. 9 which consists of DDFS for the carrier signal at frequency f_{CAR}, DDFS for the modulation signal at frequency F_{MOD}, and amplitude modulator contains two multipliers and one adder. This diagram allows choosing the carrier signal frequency, modulation signal frequency, and modulation factor in digital form, where the codes of carrier signal and modulation signal are computed according to the following mathematical relation [7]:

$$CODE\ \mathrm{f_{CAR}} = L_{CAR} = \frac{f_{CAR}.2^n}{F_{CLK}} \quad (6)$$
$$CODE\ F_{\mathrm{MOD}} = L_{MOD} = \frac{F_{MOD}.2^n}{F_{CLK}}$$

Where:
n: the DDFS accumulator capacity which define the step of synthesizer tuning.
F_{CLK}: the clock pulses frequency of the DDFS.
(f_{CAR}, F_{MOD}): the carrier signal frequency, and modulation signal frequency.
The carrier signal is considered as a sinusoidal signal of frequency f_{CAR} is changeable within a definite frequency range.

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The modulation signal is considered as a sinusoidal signal of frequency F_{MOD} is changeable within a definite frequency range.

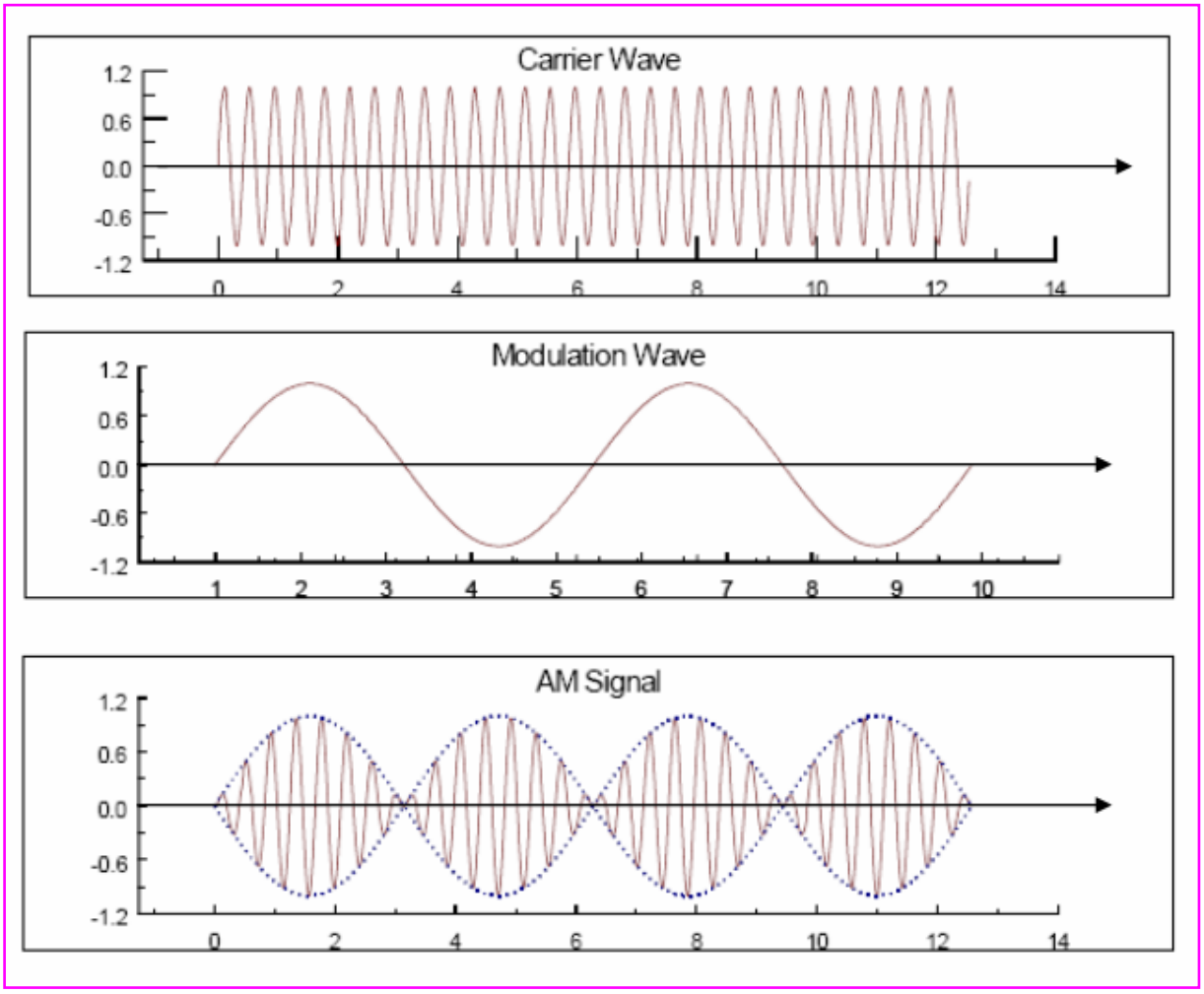

Fig. 5: The time diagram of the digital AM modulator signals

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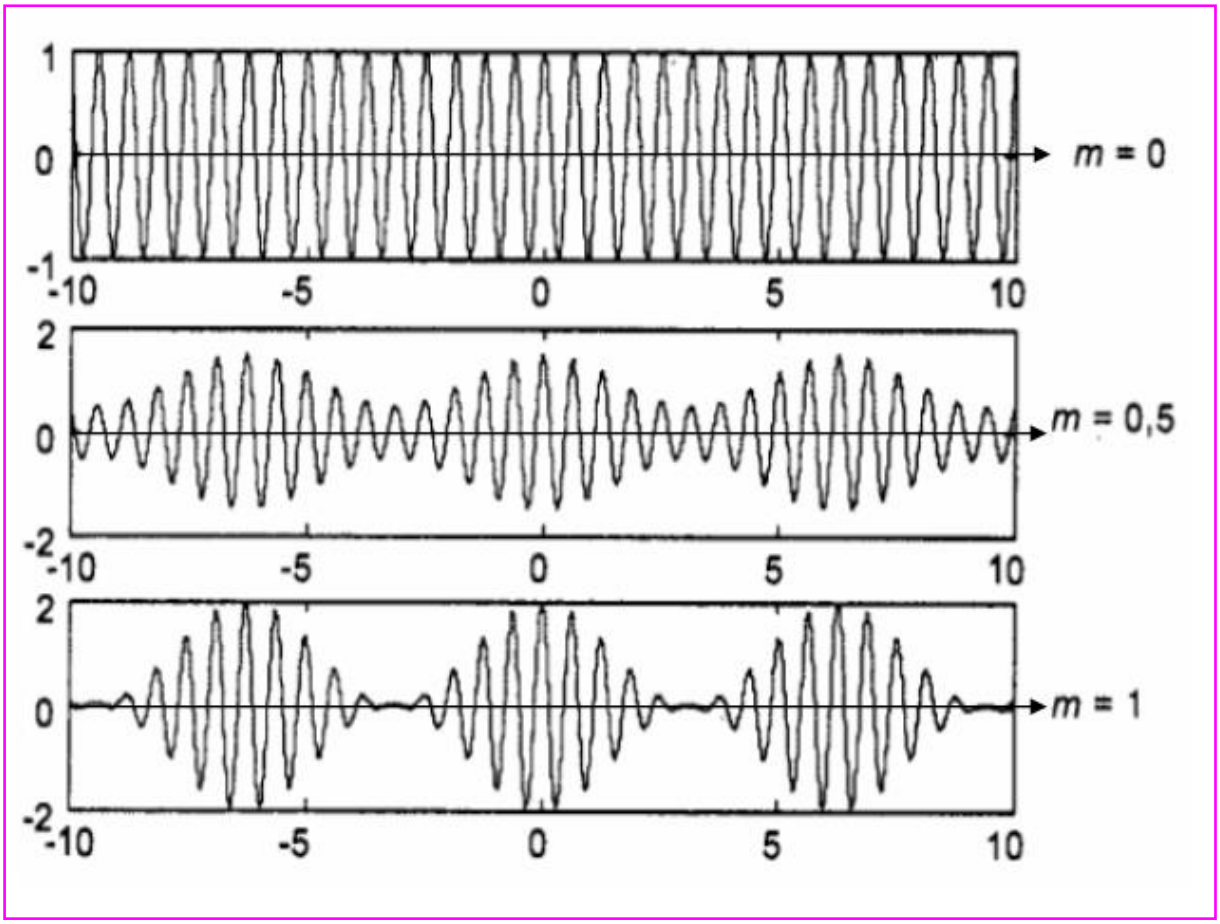

Fig. 6: The time diagram of the digital AM modulator operation for $(m = 0, m = 0.5, m = 1)$

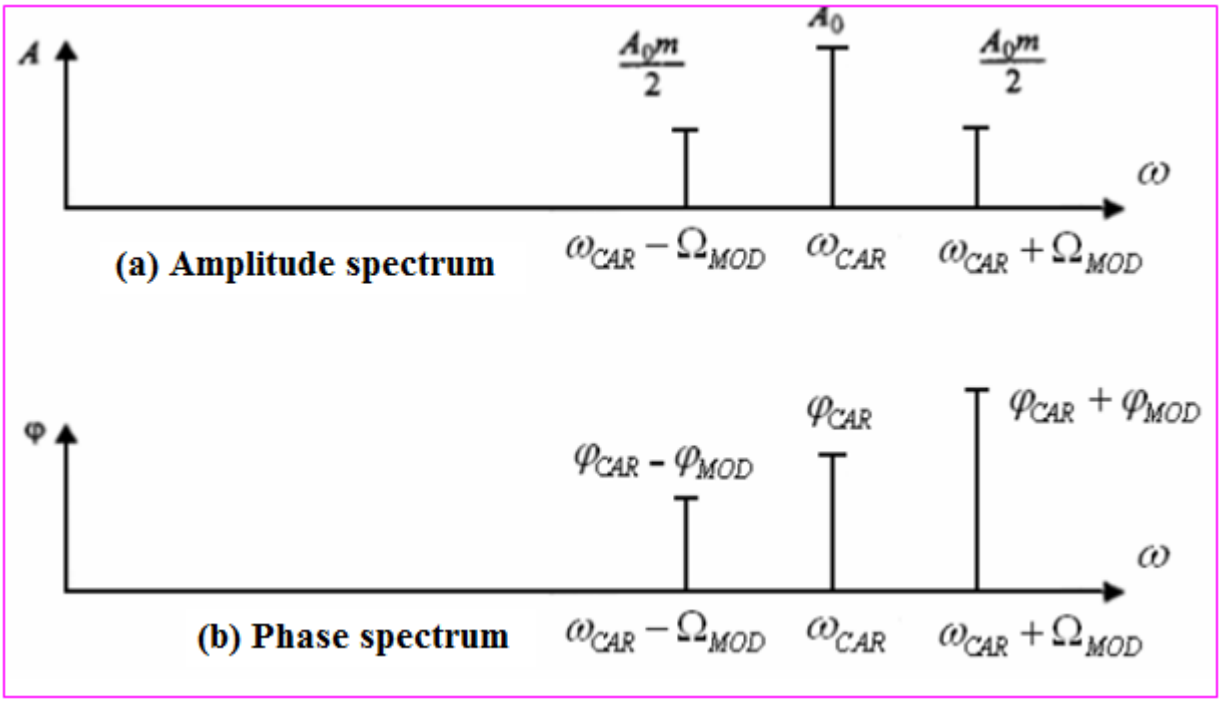

Fig. 7: The spectrum of the AM signal: a. amplitude spectrum, b. phase spectrum

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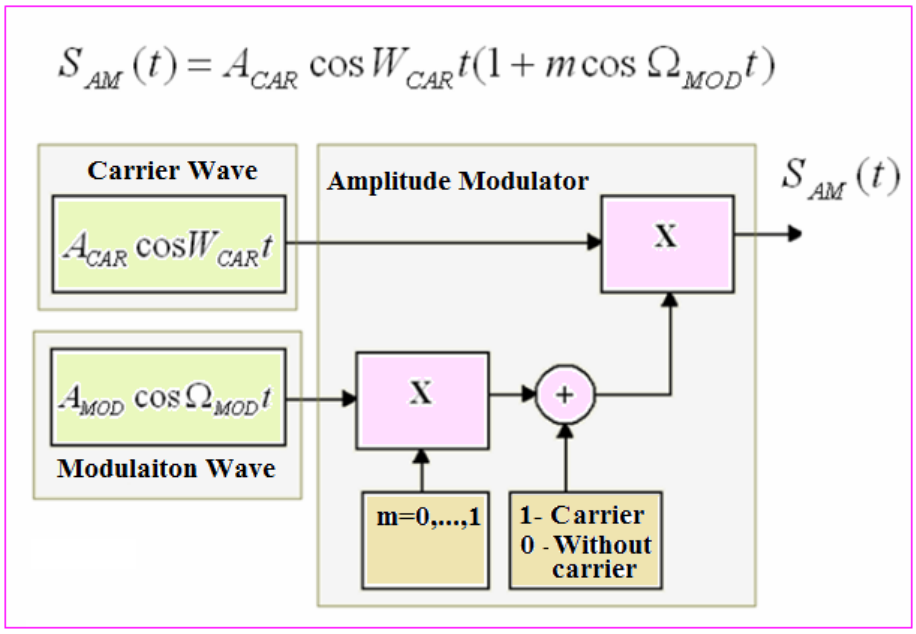

Fig. 8: The block diagram of the digital AM algorithm using DDFS

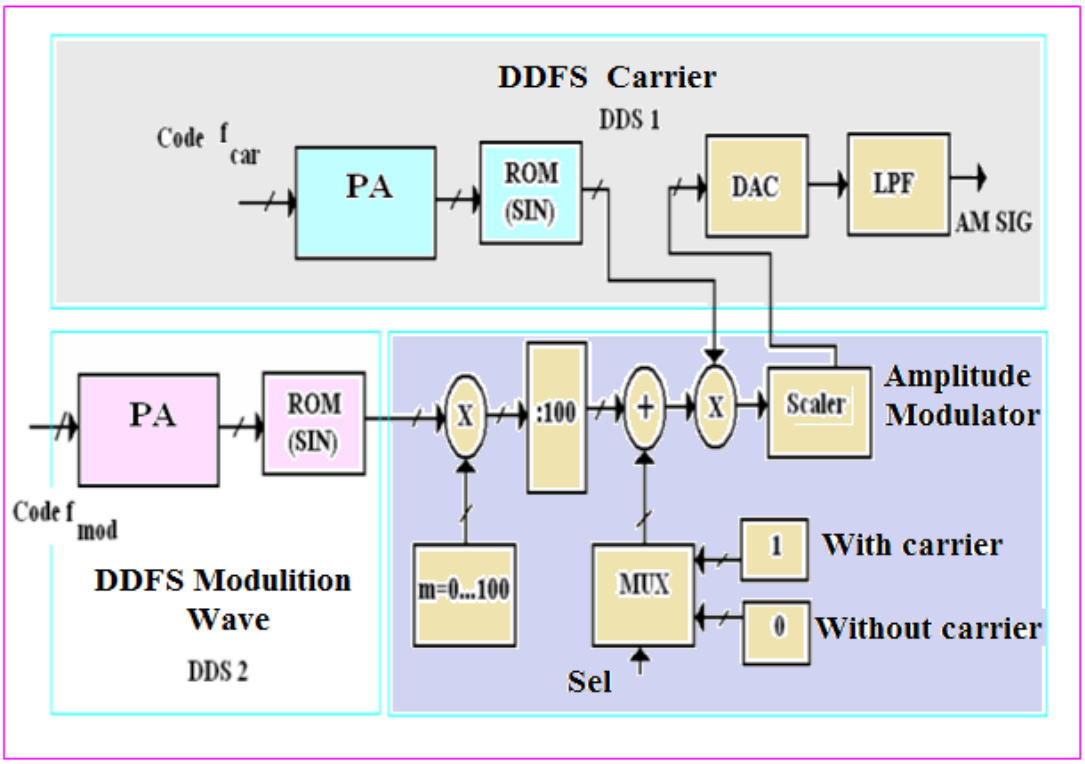

Fig. 9: The functional diagram of the digital AM algorithm using DDFS

V. THE DESIGN STAGES OF THE DIGITAL AM

1- Computing the frequency range of the DDFS.
2- Computing the number of the accumulator bits beginning with the required frequency step.
3- Computing the frequency codes for the carrier signal and modulation signal (Code f_{CAR}, Code F_{MOD}).
4- Computing the parameters of the amplitude modulator (modulation factor, with carrier or without)
5- Designing the digital AM modulator circuit using digital chips FPGA within the designing programming environment Quartus II 9.1.
-The number of the accumulator bits is computed from the following mathematical relation [8]:

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$$\delta f = \frac{F_{CLK}}{2^n} \Rightarrow 2^n = \frac{F_{CLK}}{\delta f} = \frac{50*10^6}{3} \Rightarrow n = 24bit$$

-The frequency range for the carrier and modulating signals synthesizer is computed from the following mathematical relation:

$$\Delta f = 0.... \frac{F_{CLK}}{2} = 0....25MHz$$

-To synthesis two signals of frequencies $f_{CAR} = 1MHz, F_{MOD} = 10KHz$, the frequency codes must be:

$$CODE\ \mathrm{f_{CAR}} = L_{CAR} = \frac{f_{CAR}.2^n}{F_{CLK}} = \frac{1*2^{24}}{50} = 335544$$

$$CODE\ F_{\mathrm{MOD}} = \mathrm{L_{MOD}} = \frac{F_{MOD}.2^n}{F_{CLK}} = \frac{0.01*2^{24}}{50} = 3355$$

-Modulation factor: the modulation factor is realized through multiplying the modulation signal samples by the value (m=0…100), then dividing by constant 100.
-Carrier type: the carrier type is chosen through passing the value (Y=0) in case of no carrier, or the value (Y=1) in case of carrier through the multiplexer to the adder of modulation signal samples, then the basic mathematical relation of the AM is realized in digital form:

$$S_{AM}(i) = S_{CAR}(i)*[Y + (m/100)*S_{MOD}(i)]$$
$$m = 0...100$$
$$\mathrm{Y} = 0 \quad \mathrm{OR}\ 1$$
$$Y = 0 \Rightarrow S_{AM}(i) = S_{CAR}(i)*(m/100)*S_{MOD}(i) \qquad (7)$$
$$Y = 1 \Rightarrow S_{AM}(i) = S_{CAR}(i)*[1 + (m/100)*S_{MOD}(i)] =$$
$$= S_{CAR}(i) + S_{CAR}(i)*(m/100)*S_{MOD}(i)$$

Where: (i) the sample number, $S_{CAR}(i)$ carrier signal samples, $S_{MOD}(i)$ modulation signal samples, $S_{AM}(i)$ the AM signal samples.
-The AM in digital way is considered as a multiplication, dividing, and adding operations for digital samples of the modulation signal and carrier signal according to the previous relation, so there is need to realize a synchronization for these operations through one clock pulses $F_{CLK} = 50MHz$, for all operations as shown in the figure. 10 , figure. 11, figure. 12, figure. 13, figure. 14.

-The result of multiplication, adding, subtracting, and dividing for positive and negative samples is a large number out of the required words length limits, and sometimes take places a redundancy .??? operations for these values causing a big and illogical errors in these operations. So there is need to make a scaling operation where we obtain values within the required ranges in all digital modulation stages through dividing, multiplication, adding, and subtracting of the operations and this what realize it the scaling algorithm.
-The modulation factor is measured through the time diagram of the AM signal shown on the oscilloscope according to the following mathematical relation:

$$m = \frac{U_{MAX} - U_{MIN}}{U_{MAX} + U_{MIN}} * 100 \qquad (8)$$

The general functional diagram of modulator AM_MOD using the programming environment Quartus II 9.1 is shown in figure. 10 due to $f_{CAR} = 1MHz, F_{MOD} = 10KHz$ and it consists of:

-The modulation signal synthesizer DDS_MOD.
-The carrier signal synthesizer DDS_CAR.
-Amplitude modulator AM_MODULATOR.
-Clock pulses generator of frequency $F_{CLK} = 50MHz$ for all components of the digital amplitude modulator.
-Scaling algorithm.

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Figure. 11 shows the detailed diagram of the modulation signal synthesizer which is considered as a DDFS. figure. 12 shows the detailed diagram of the carrier signal synthesizer. figure. 13 shows the detailed diagram of the amplitude modulator which is considered as a set of multipliers and dividers of the modulation signal and carrier signal samples. figure. 14 shows the scaling algorithm.

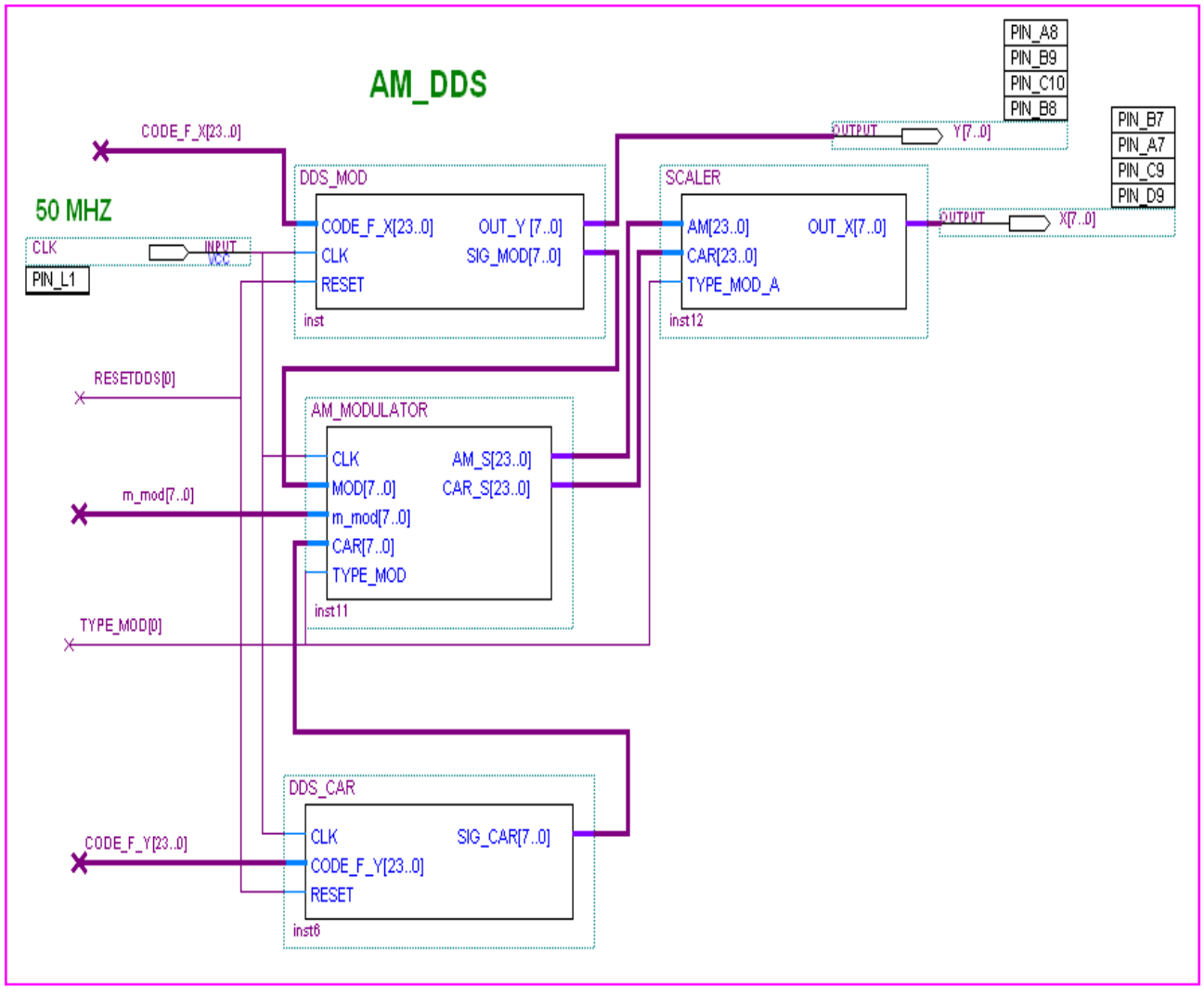

Fig. 10 The general functional diagram of the digital modulator AM using Quartus II 9.1

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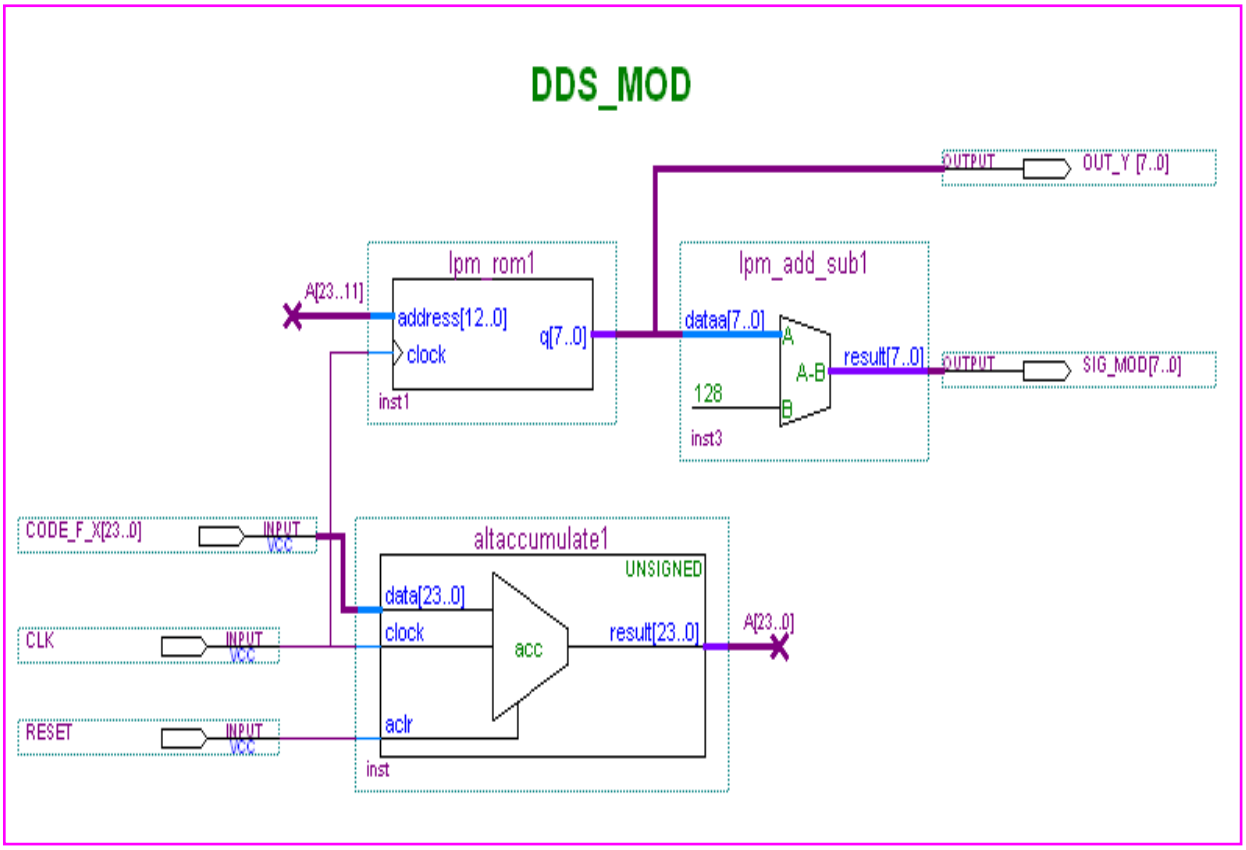

Fig. 11: The detailed diagram of the modulation signal synthesizer using Quartus II 9.1

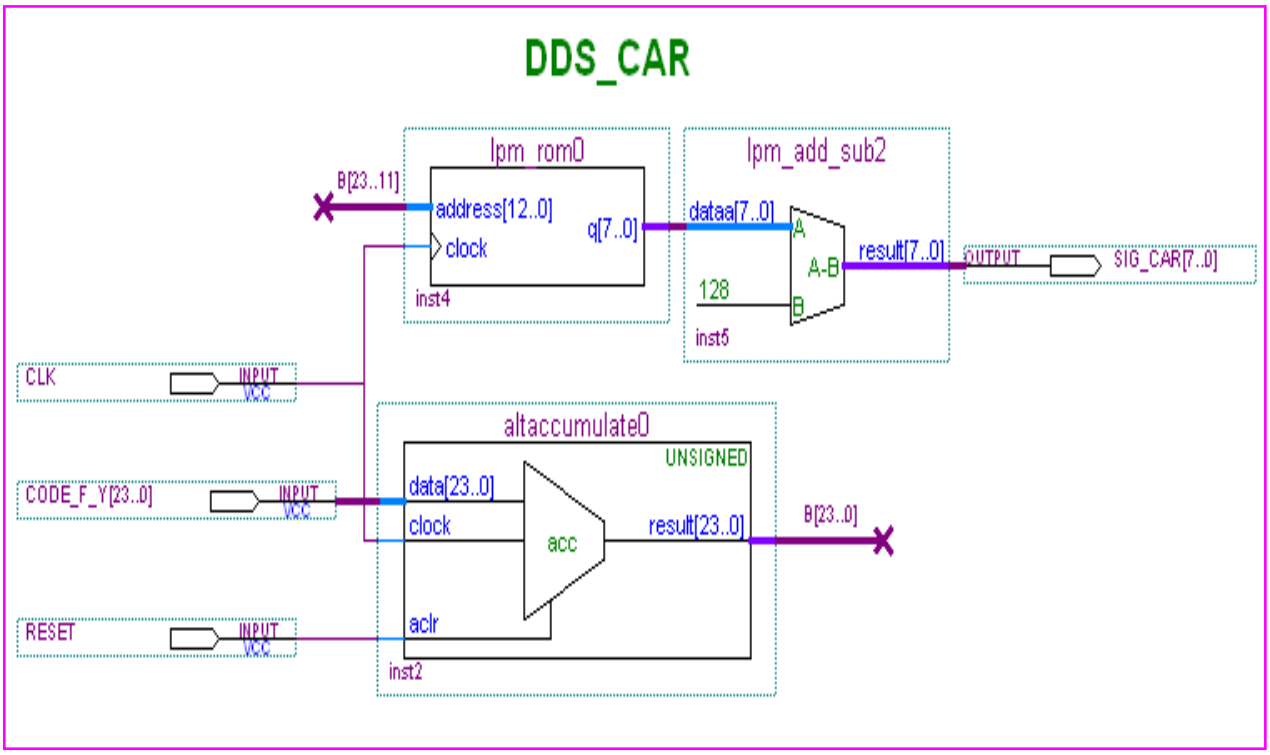

Fig. 12: The detailed diagram of the carrier signal synthesizer using Quartus II 9.1

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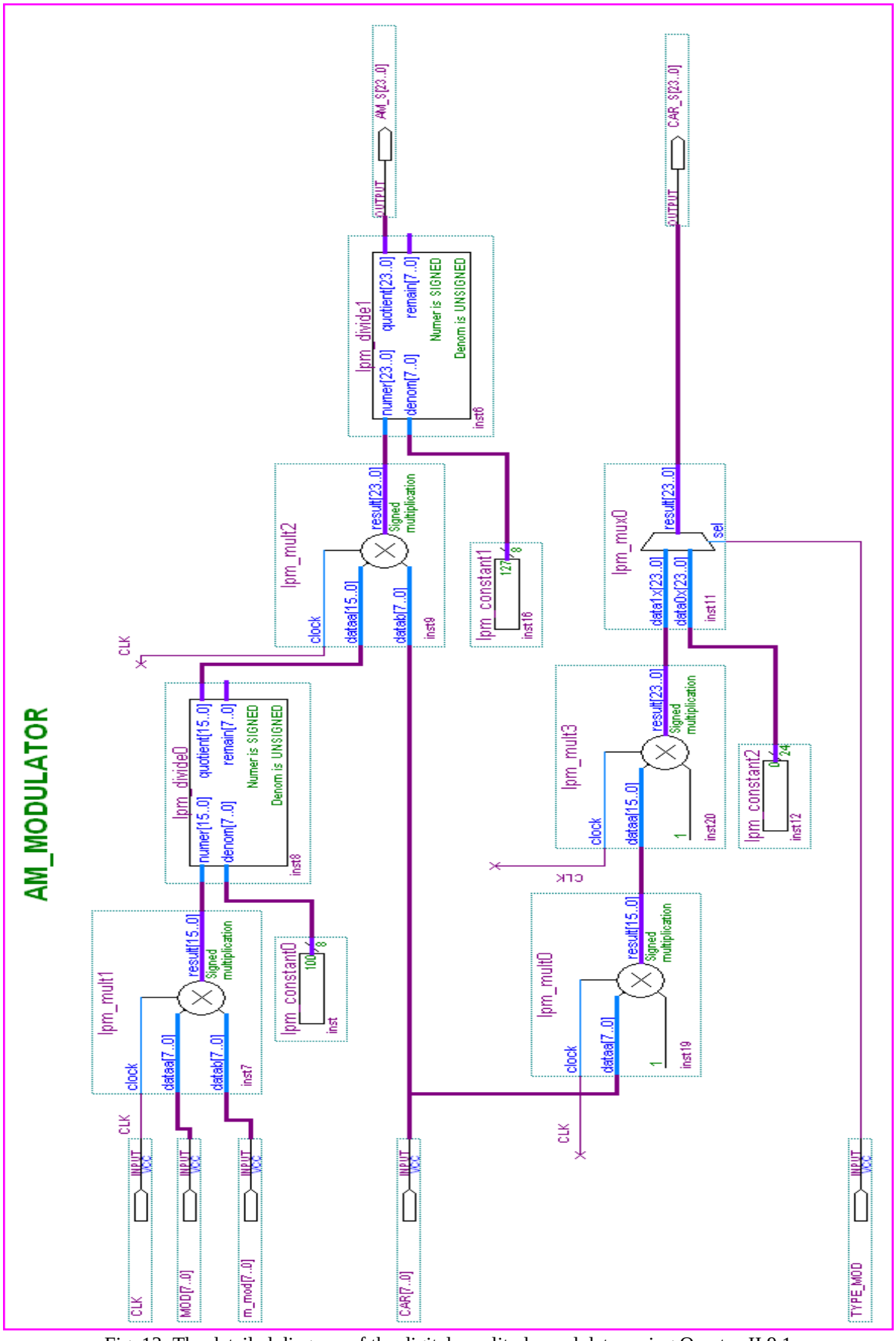

Fig. 13: The detailed diagram of the digital amplitude modulator using Quartus II 9.1

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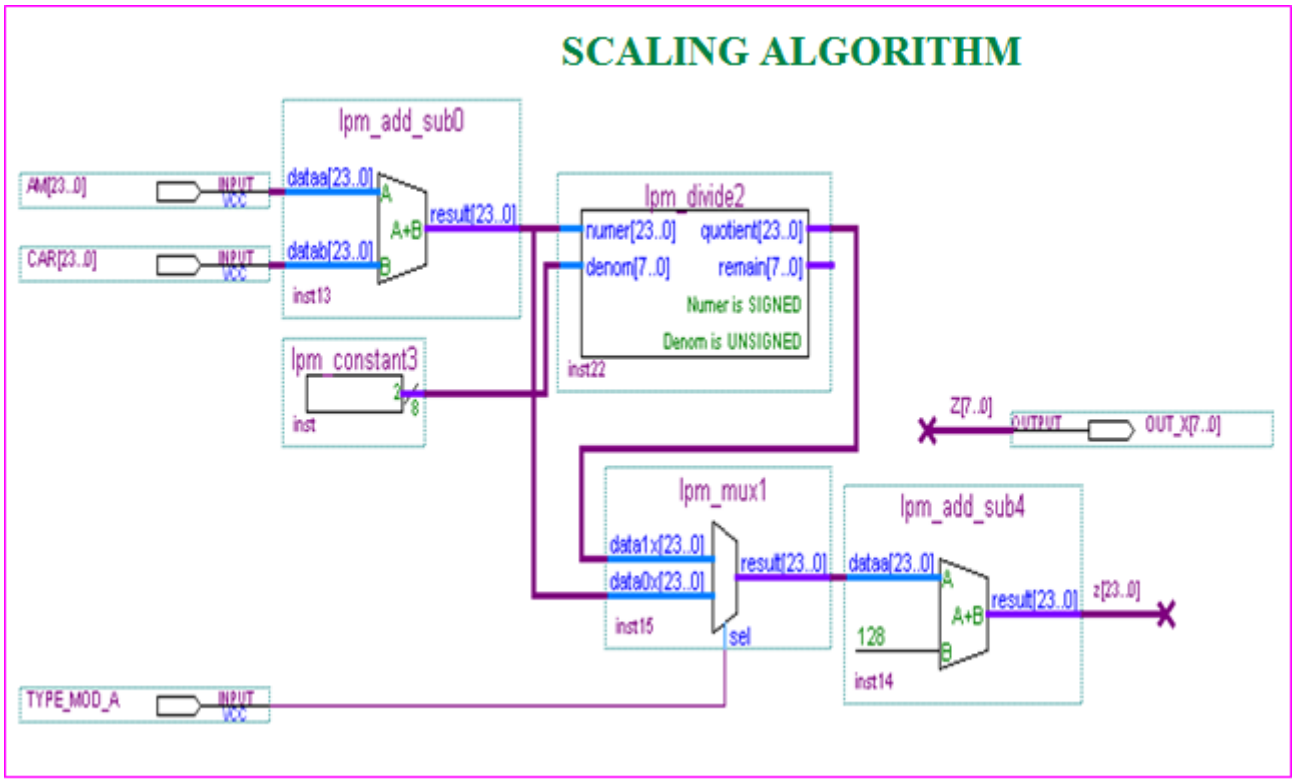

Fig. 14: The detailed diagram of the scaling algorithm using Quartus II 9.1

VI. RESULTS OF DESIGN

The results of the practical design of the digital AM modulator in time domain due to different values of (m) using the FPGA chip are shown in figures .15. The results of the previous design in frequency domain due to different values of (m) are shown in figures .16.

These figures are taken from screen of digital oscilloscope, and digital spectrum analyzer. We note from the practical results the identification between the theoretical results and the practical results which indicate the high accuracy of digital synthesizing and modulation operations for these signals.

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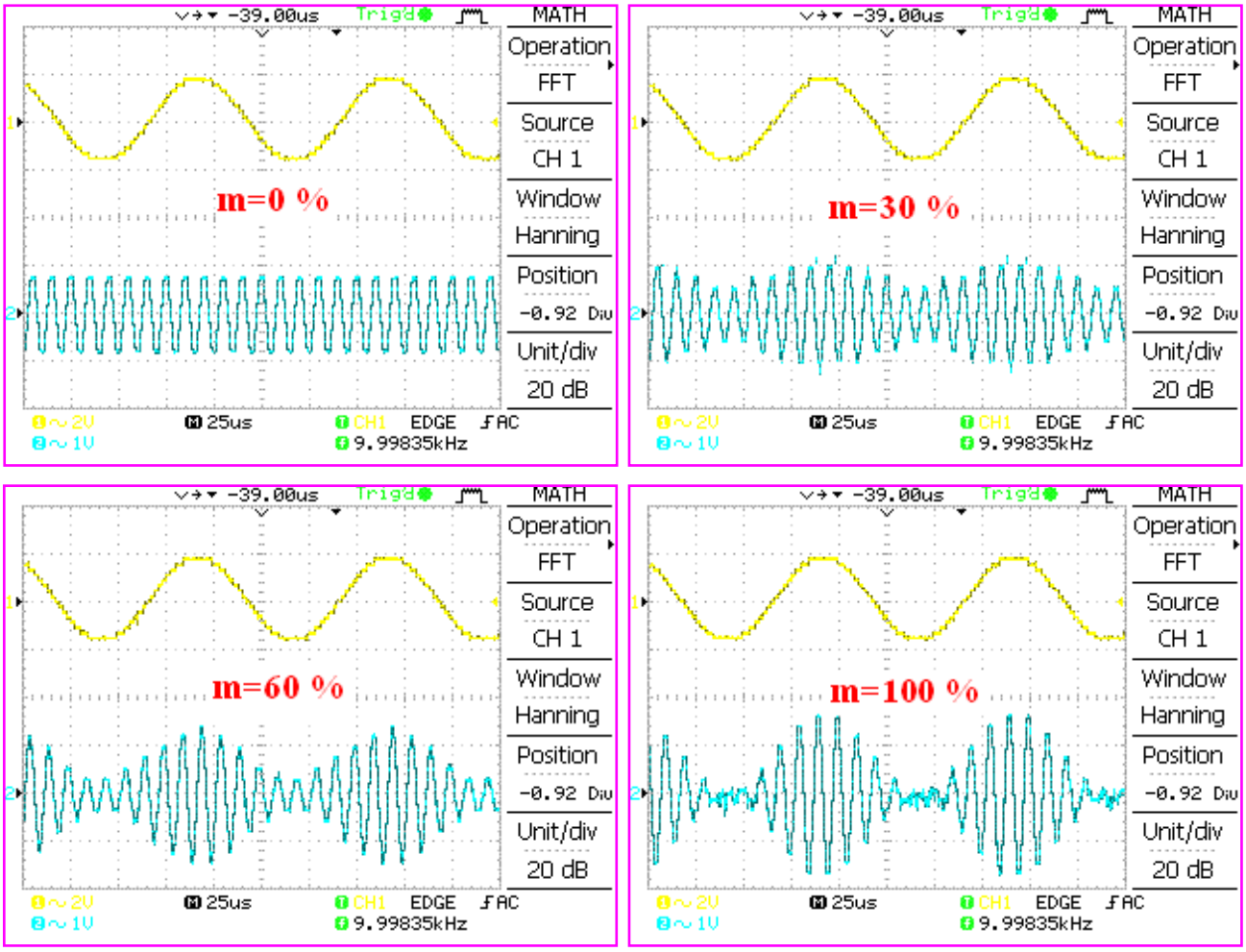

Fig. 15: The practical results of the AM modulator in time domain due to different values of m

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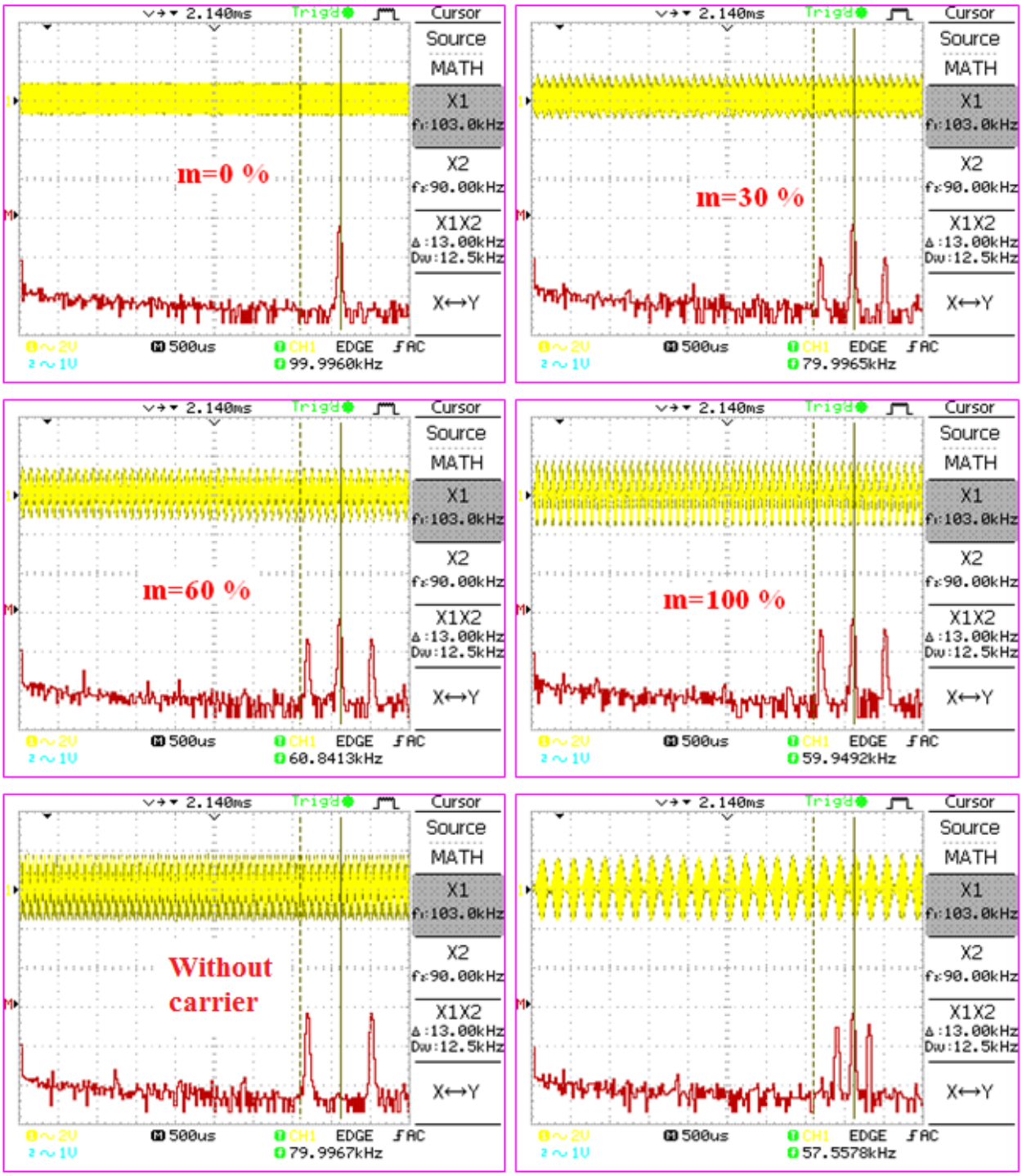

Fig. 16: The practical results of the digital AM modulator in frequency domain due to different values of m

VII. DISCUSSION AND CONCLUSION

-Using DDFS techniques in communication domain allows implementing different digital modulation operations (AM, FM,PM,SSB etc) with high accuracy and speed in digital signal synthesizing, and with the ability of changing parameters in wide range.
-Using DDFS techniques in communication domain allows implementing the digital processing in the communication receiver on high intermediate frequency.
-We note from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital synthesizing and modulation operations for signals.
-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).

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-The most important thing in this paper is the possibility of changing the frequency of the modulation signal, and the frequency of the carrier signal.

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BIOGRAPHY

Dr. Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR , university of communication in Leningrad , holds a degree assistant professor in 2009 from Aleppo university.
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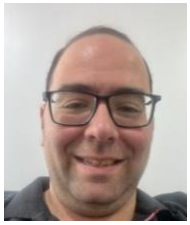
Publish a lot of research in the field of digital communication and digital signal processing in the universities journals of Syria and in the European and Indian journals.
Working in the field of programming FPGA by using VHDL and design of Digital Filters.



Dr. Abdul-Aziz Shokyfeh holds a PhD in telecom engineering in 2017 from Damascus Syria, Faculty of Mechanical and Electrical Engineering Telecommunication and electronic department .
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Dean of IT college at Ittehad Private University, from 2023 till now.
Publish a lot of research in field of antenna in Syrian and European journals .Working in field of PBXs , Network , low current system and solution.

Dr. Amer Garib holds a PhD in communication engineering in 1994 from the USSR, university of communication in Leningrad. Lecturer at Department of Faculty of Informatics Engineering , Ittihad Private University- Syria.
Publish a lot of research in the field of digital communication in the universities of Syria and in the Indian journals. Working in the field of Digital Communication System