International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

Design and Implementation of a Digital Liner Frequency Modulation (LFM) Synthesizer using FPGA

Dr. Kamal Aboutabikh[1], Dr. Abdul-Aziz Shokyfeh[2], Dr. Amer Garib[3]

Faculty of Informatics Engineering, Ittihad Private University, Damascus- Syria [1,2,3]

Abstract:
This paper proposes the design and implementation mechanism of digital LFM synthesizer, based on the use of Direct Digital Frequency Synthesizer (DDFS). The proposed synthesizer is achieved using Cyclone II EP2C20F484C7 FPGA, placed on education and development board DE-1.
Using DDFS techniques in radar domain allows implementing different digital modulation operations (pulse, LFM, BPSK according to Barker codes, coherent and etc) with high accuracy and high speed in digital signal synthesizing.
The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).

Keywords: Digital Modulator LFM , DDFS, FPGA.

INTRODUCTION

Linear frequency modulation signals are widely used in radar technology because they have the feature of increasing the pulse width in the transmitter to increase the radar range, and compressing the pulse in the receiver to achieve high range-resolution.
In this paper we designed and implemented the mechanism of digital synthesizing for LFM pulses with increased, and decreased frequency modulation, using a digital programmable device (Cyclone II EP2C20F484C7 FPGA from ALTERA), placed on education and development board DE1. The proposed synthesizer has the following parameters**:**
-Modulation type of signal is: LFM according to the law of increasing and decreasing frequency.
-The frequency range within the pulse width is variable up to the range (1.5….5) MHz.
-The width range of pulse is variable up to the range (10…30) us.
-Base of LFM signal: is variable up to the range:

$$\{B = \Delta f . \tau = 15 \ldots .150\}$$

- repetition time of pulses: 100 usec.
-Step Rate Clock: F_{STEP}=1 MHz or T_{STEP}=1/F_{STEP} =1 us.
-Number of steps: ($N = \frac{\tau}{T_{STEP}} = \frac{10}{1} . \ldots \frac{30}{1} = 10 \ldots .30$)
-The fraction frequency shift value is: ($df = \frac{\Delta f}{N} = \frac{1.5}{10} \ldots \frac{5}{30}\ MHz = 150KHz \ldots .167\ KHz$)
-All variable parameters are computer – controlled, with LFM or without LFM
(f_{START} , f_{STOP} , $N, \Delta f$, df , τ , $T, B,$ direction of LFM (increased or decreased),)

The parameters of the LFM generated signal are analyzed using a digital oscilloscope and spectrum analyzer GDS-1052U.
The LFM signal is given according to the following mathematical relation [1]:

International Multidisciplinary Research Journal Reviews (IMRJR)
International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

$$S_{LFM}(t) = A_0 \cos\left(\omega_0 t + \frac{\eta . t^2}{2}\right) \quad , \quad 0 < t \le \tau$$

$$\eta = \frac{\Delta\omega}{\tau} = \frac{2\pi.\Delta f}{\tau} \Rightarrow$$

$$S_{LFM}(t) = A_0 \cos\left(\omega_0 t + \frac{\Delta\omega . t^2}{2.\tau}\right) \quad , \quad 0 < t \le \tau \qquad (1)$$

Where:

(A_0): Amplitude of LFM signal.

$(w_0 = w_{START})$: Start frequency of LFM signal.

$(\Delta f = f_{STOP} - f_{START})$ or $(\Delta w = 2\pi\ \Delta f)$: Is considered as a frequency shift value within the pulse width.

(τ) : Pulse width.

$(\eta = \frac{\Delta f}{\tau})$: the speed of frequency changing through the pulse width time (τ).

The LFM signal in time domain is shown in figure (1) in case of increased continues LFM.

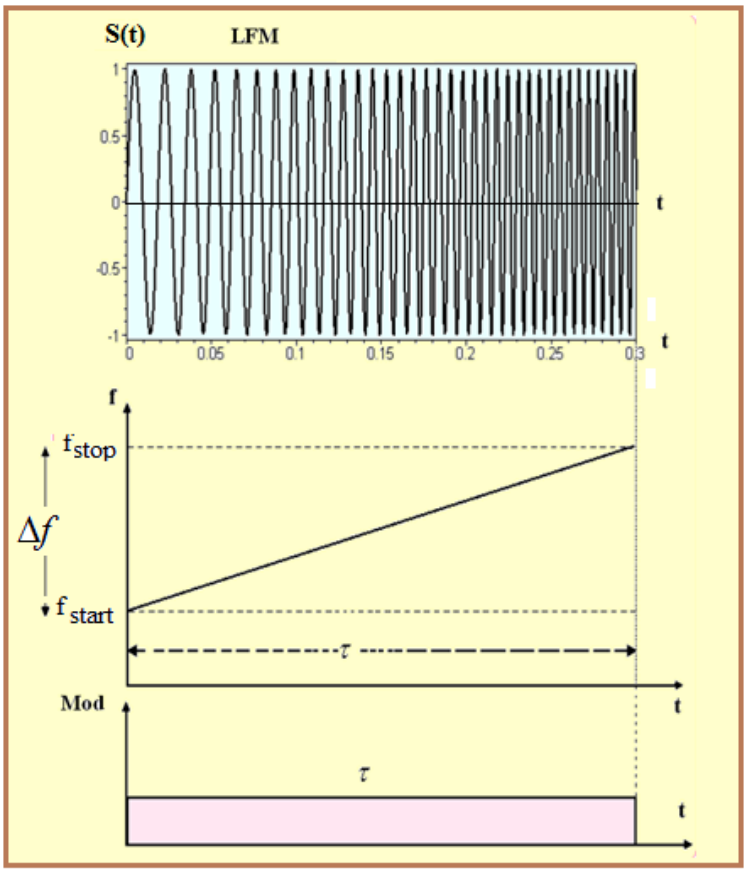

Fig. (1): continues modulating signal, and LFM signal

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

The mathematical principle of digital LFM using DDFS can be explained according to the diagram shown in figure (2). The LFM synthesizer is achieved by accumulating the value of (df) code with the value of start frequency code $(Code\ f_{START})$ every (T_{STEP}) to read the stored sinusoidal samples in ROM of DDFS [2].

The stored values of the sine signal in ROM of DDFS is calculated according to the following equation [2]:

$$U_{\sin}(i) = INT\left[\left(2^{m-1}-1\right).\sin\left(\frac{360.i}{2^{b}}\right)\right] \qquad (2)$$

For:

$$\mathrm{m} = 8\,\mathrm{bits}\,,\ \mathrm{b} = 14\,\mathrm{bits}\,,\ i = (0....2^{b}-1) = (0...16383)$$

Then:

$$U_{\sin}(i) = INT\left[\left(2^{8-1}-1\right).\sin\left(\frac{360.i}{2^{14}}\right)\right] = INT\left[127.\sin\left(\frac{360.i}{16383}\right)\right]$$

$$U_{\sin}(i) = (-127..... +127)$$

To avoid negative values that are difficult to store in memory, we add a value off-set= 128, then

$$U_{\sin}(i) = (0.....255)$$

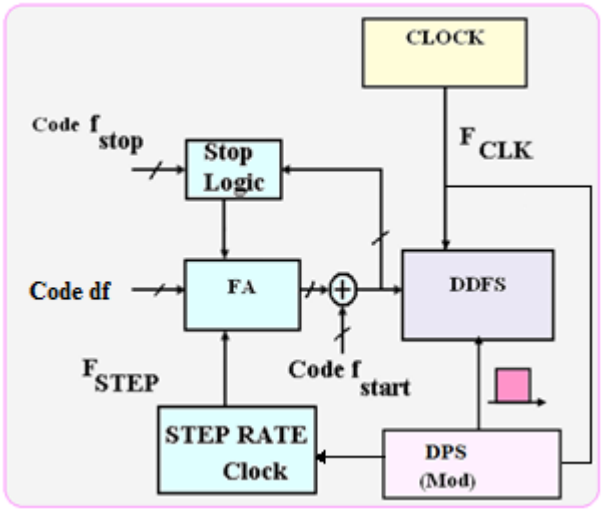

Fig (2): The block diagram of the LFM synthesizer using DDFS

Paper [3] presents the simple method of design and implementation of a LFM (linear frequency modulation) waveform or chirp of (3 µsec) pulse duration using DDFS (AD9858), but in this paper the width range of pulse is variable up to the range (10…30) µsec.

Paper [4] presents the design and implementation of a LFM waveform or chirp of (4 µsec) pulse duration of a LFM using DDFS (AD9914) but in this paper the width range of pulse is variable up to the range (10…30) µsec.

II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

-In this paper digital LFM synthesizer was designed, implemented, and tested based on the use of Digital Direct Frequency Synthesizer (DDFS) using FPGA, VHDL and Graphical programming language with Quartus II 9.1 design environment.
-Using the digital DDFS with mathematical operations (adding, multiply, division), makes the digital modulation design process flexible, accurate and highly efficient.
-Changing the parameters of pulse signals (signal (width and period), carrier frequency, direction of LFM, and frequency deviation shift explains the difference between digital modulation and analog modulation.

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the digital modulators for different modulation types of signals, the following tools and software are used:

-Cyclone II EP2C20F484C7 FPGA chip from ALTERA (with highly accuracy, speed, and level specifications) placed on education and development board DE-1 [5].
-DDFS which is considered as highly accuracy technique in sinusoidal and square signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment [6].
-Design Environment MATLAB R2008a.
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [7] is shown in figure (3).

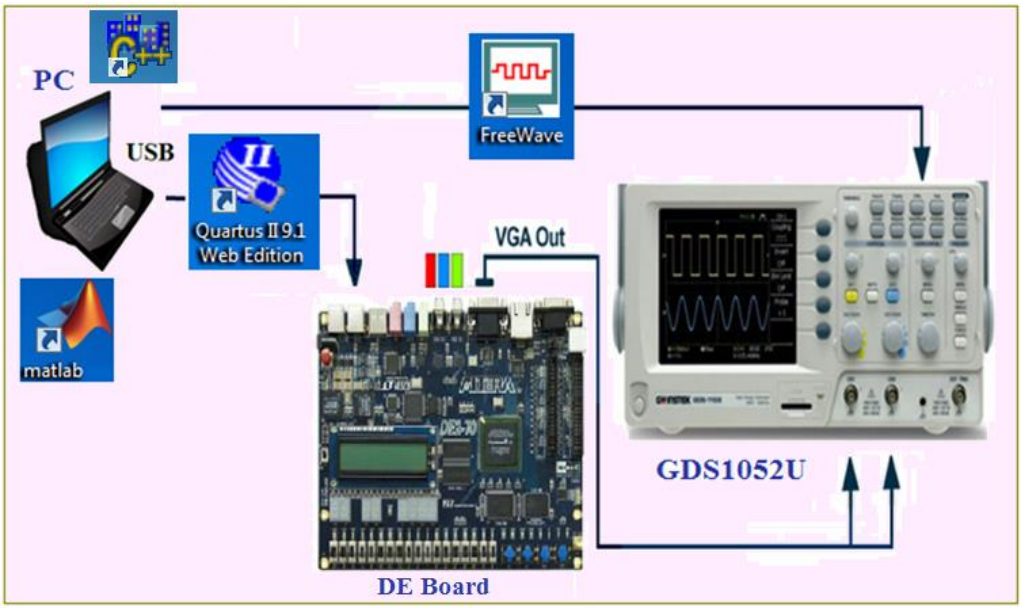

Figure (3) Block diagram of the laboratory experiment platform

IV. THE FUNCTIONAL DIAGRAM OF DIGITAL LFM SYNTHESIZER

The time diagram of the LFM signal is shown in figure (4) in case of increased LFM [9] , and is shown in figure (5) in case of decreased LFM. The LFM is implemented using DDFS according to the functional diagram shown in the figure (6) in case of increased LFM, which consists of DDFS, the pulse modulating signal synthesizer (Mod), the LFM signal synthesizer which consists of frequency accumulator (FA) of input value (df), the increased LFM step pulses generator (Step Rate Clock) of frequency ($F_{STEP}=1/T_{STEP}$), modulation stop circuit (Stop logic) which stops the frequency accumulating operation when the accumulating value (df) equals the value of the end frequency (F_{STOP}), adder circuit to add the start frequency to the accumulating value.
The functional diagram of the LFM in case of decreased LFM modulator is shown in the figure (7). In case of decreased LFM, the stop circuit (Stop logic) which stops the frequency accumulating operation when the accumulating value (df) equals the value of the start frequency (F_{START}), subtracter circuit to subtract the start frequency from the accumulating value (df).
The main difference between the two cases is done in the mathematical algorithm structure as shown in the previous relations. The following frequency codes $(f_{START}, f_{STOP}, \Delta f = f_{STOP} - f_{START}, df = \Delta f / N)$ are computed according to the following mathematical relations [2]:

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

$$Code\,\mathrm{f}_{\mathrm{START}} = L_{START} = \frac{f_{START}.2^n}{F_{CLK}}$$

$$Code\,\mathrm{f}_{\mathrm{STOP}} = L_{STOP} = \frac{f_{STOP}.2^n}{F_{CLK}} \qquad (3)$$

$$\mathrm{Code}\ df = \frac{df.2^n}{F_{CLK}} = \frac{\Delta f.2^n}{N.F_{CLK}}$$

Where:

n: is the capacity of the DDFS accumulator which defines the synthesizer tuning step.

F_{CLK} : the clock pulses frequency of the DDFS.

(f_{START}, f_{STOP}) : the start and stop frequencies for the LFM synthesizer signal.

$\Delta f = (f_{STOP} - f_{START})$: the value of the frequency shift for the LFM signal.

N: an integer number expresses the number of generator pulses STEP RATE CLOCK and expresses the pulse width according the following relation [2]:

$$\tau = NT_{STEP} \Rightarrow N = \frac{\tau}{T_{STEP}} = \frac{\Delta \mathrm{f}}{\mathrm{df}} \qquad (4)$$

The frequency modulation speed (the speed of frequency changing) within the pulse width is expressed according the following relation [8]:

$$\eta = \frac{2\pi.\Delta f}{\tau} = \frac{2\pi.df.N}{\tau} = \frac{2\pi.df.(\frac{\tau}{T_{STEP}})}{\tau} = \frac{2\pi.df.\tau}{\tau.T_{STEP}} = \frac{2\pi.df}{T_{STEP}} \qquad (5)$$

(η) must be change in case of changing $\Delta f = (f_{STOP} - f_{START})$ or in case of changing (τ), the value of (T_{STEP}) always be $(T_{STEP} = CONST)$, while the value (df) is changed according to change $\Delta f = (f_{STOP} - f_{START})$ and (τ).

International Multidisciplinary Research Journal Reviews (IMRJR)
International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

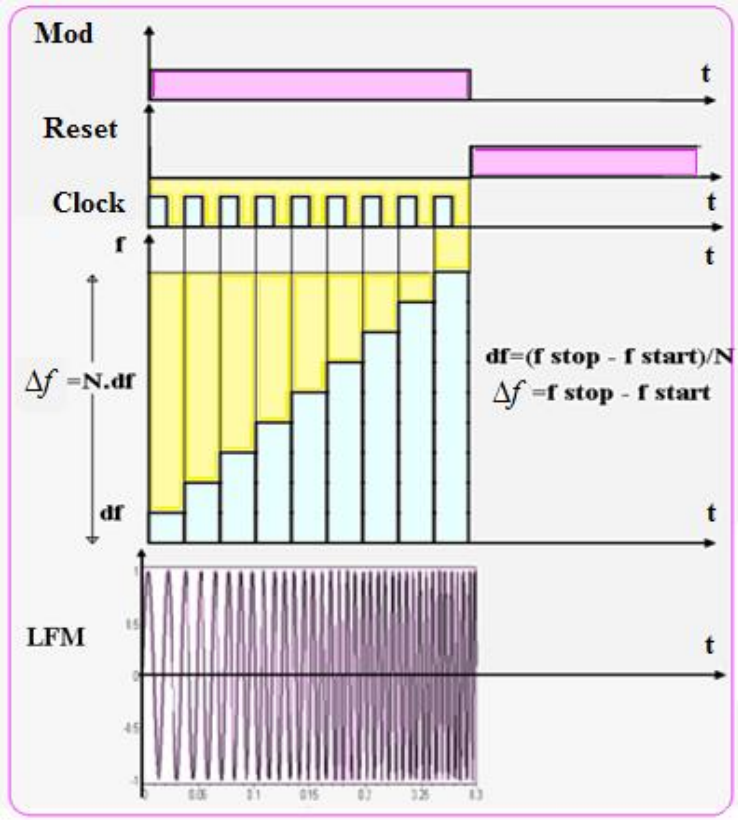

Fig. (4): Modulating signal, and LFM signal in case of increased frequency

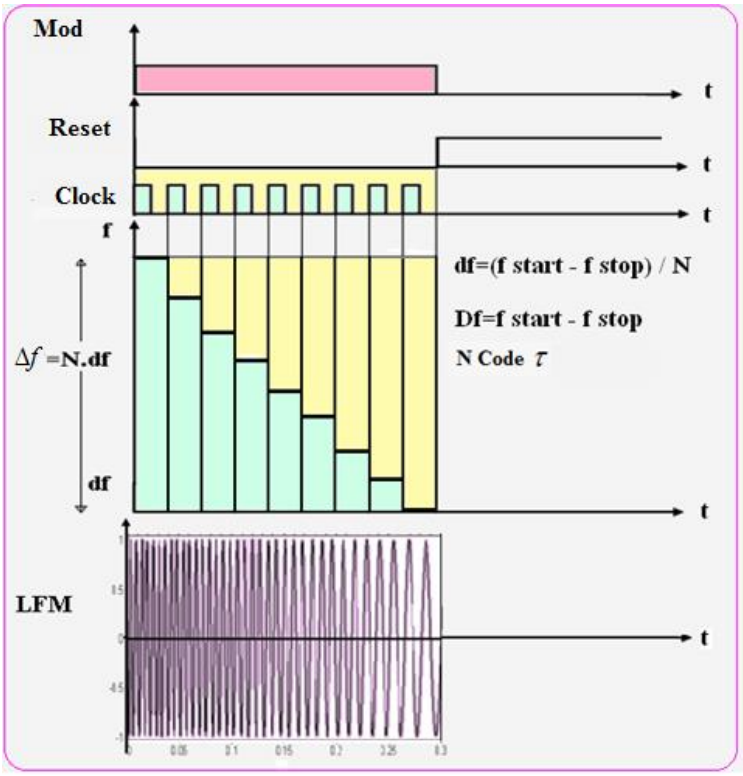

Fig. (5): Modulating signal, and LFM signal in case of increased LFM

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

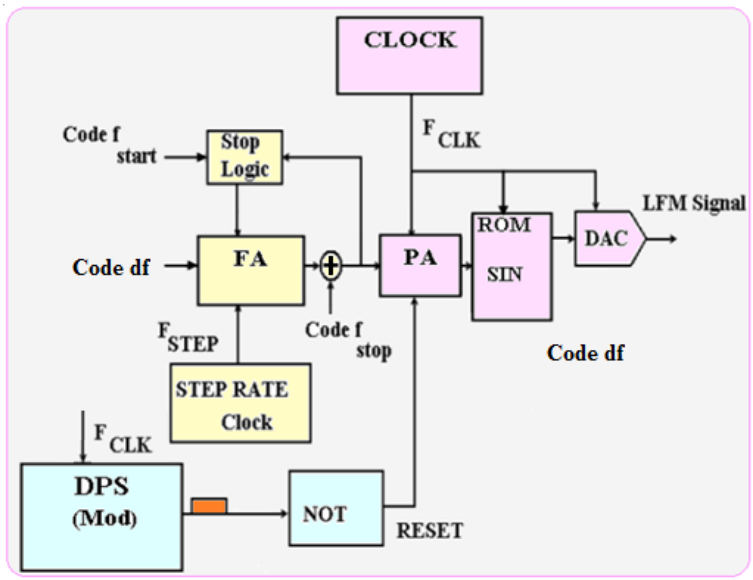

Fig. (6): The functional diagram of the LFM synthesizer in case of increased LFM

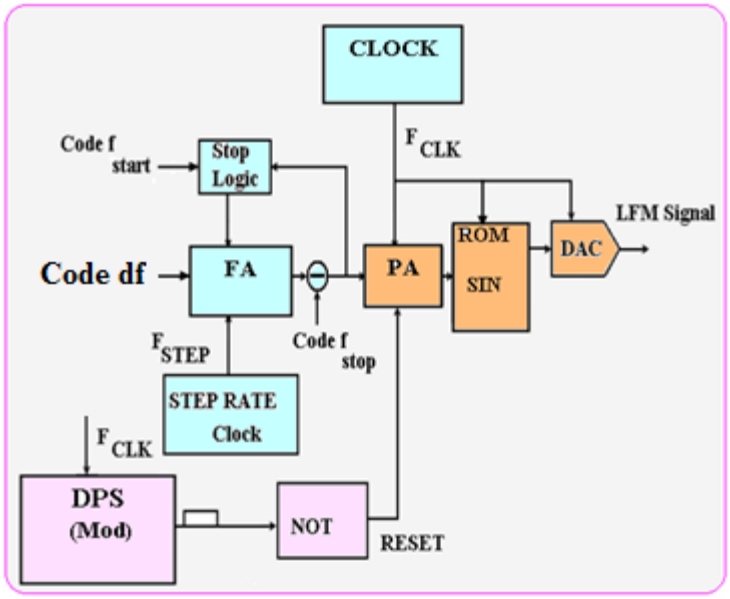

Fig. (7): The functional diagram of the LFM synthesizer in case of decreased LFM

V. THE DESIGN STAGES OF THE DIGITAL LFM SYNTHESIZER

1.Computing the frequency range of the DDFS.
2.Computing the number of accumulator bits depending on the required frequency step.
3.Computing the frequency codes (Code f_{START} , Code f_{STOP} , Code Δf , Code df).
4.Computing the parameters of modulating signal synthesizer (Mod).
6.Designing the digital LFM synthesizer circuit using digital chips FPGA within the designed programming environment Quartus II 9.1.

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

Practical design of digital LFM synthesizer:

We have a DDFS which has the following parameters:

-The frequency resolution of the LFM synthesizer is: $(\delta f = 0.011Hz)$, $F_{CLK} = 50MHz$, $F_{STEP} = 1MHz$ -The modulation law is: increased LFM, decreased LFM.

-The repetition time and width of pulse modulation (Mod) is: $(T = 100\mu s)$ and $(\tau = 20\mu s)$ (this value is chosen for easy computing).

-The ROM memory capacity for the stored signal samples is 16384x8 bit and their values are positive within the range (0…..255).

-The number of accumulator bits is computed from the following relation:

$$\delta f = \frac{F_{CLK}}{2^n} \Rightarrow 2^n = \frac{F_{CLK}}{\delta f} = \frac{50*10^6}{0.0011} \Rightarrow n = 32\,bits$$

-The maximum frequency range of the synthesizer: $\Delta f = 0....\frac{F_{CLK}}{2} = 0....25MHz$.

- For frequency range (f_{START}=0.5MH, f_{STOP}= 2MHz), then The frequency shift value is:

$\Delta f = f_{STOP} - f_{START} = 2000 - 500 = 1500KHz$

- Step Rate Clock: F_{STEP}=1 MHz or $T_{STEP}=1/F_{STEP}$ =1 us.

- The number of chips (N) during the pulse width (pulse width code) is equal to:

$$N = \frac{\tau}{T_{STEP}} = \frac{20}{1} = 20$$

- The fraction frequency shift value is:

$$df = \Delta f / N = 1500/20 = 75KHz$$

-The speed of frequency modulation (the speed of frequency changing within the pulse width) equals to:

$$\eta = \frac{\Delta f}{\tau} = \frac{1500}{20} = 75[KHz/\mu s]$$

The frequency codes must be:

$$Code\,\mathrm{f}_{\mathrm{START}} = L_{START} = \frac{f_{START}.2^n}{F_{CLK}} = \frac{0.5*2^{32}}{50} = \frac{65536}{50} = 42949673$$

$$Code\,\mathrm{f}_{\mathrm{STOP}} = \mathrm{L}_{\mathrm{STOP}} = \frac{f_{STOP}.2^n}{F_{CLK}} = \frac{2*2^{32}}{50} = \frac{2*65536}{50} = 171798692$$

$$Code\,df = \mathrm{L}_{df} = \frac{df.2^n}{F_{CLK}} = \frac{75*2^{32}}{50000} = 6442451$$

-The pulse modulation signal Mod of repetition time $(T = 100\mu s)$ and width $(\tau = 20\mu s)$ which is obtained by digital pulses synthesizer using programmable counters for period and width.

VI. THE FUNCTIONAL DIAGRAM OF DIGITAL LFM SYNTHESIZER IN QUARTUS II 9.1

The functional diagram of digital LFM Synthesizer in Quartus II 9.1 environment is shown in figure (8). It consists of:

1- Frequency divider to obtain the Step Rate Clock with F_{STEP}=1MHz, which is designed using VHDL.

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

2- Digital Pulse synthesizer (DPS) to synthesize modulating pulses (Mod) of required period (T) and width (τ) .The functional diagram of this DPS synthesizer is shown in the figure (9), and it is designed using programmable counters. This DPS consists of pulse width synthesizer according to the detailed diagram shown in the figure (10), repetition period synthesizer according to the detailed diagram shown in the figure (11). Figure (12) shows the simulation results of the DSP synthesizer operation within the programming environment Quartus II 9.1. Figure (13) shows the designed results of the DSP synthesizer in time domain, where pulse width $(\tau = 20\,\mu\,\text{sec})$ and $(T = 100\,\mu\,\text{sec})$

3- LFM algorithm for: start frequency f_{START} = 0.5MHz (this corresponds to a frequency code of "42949673"), stop frequency f_{STOP} =2MHz (this corresponds to a frequency code of "171798692"), and frequency shift (df=75 KHz) which corresponds to a frequency code of "6442451". The functional diagram of LFM algorithm in Quartus II 9.1 design environment is shown in figure (14).

4- DDFS, the functional diagram of the DDFS in Quartus II 9.1 design environment is shown in figure (15) where output signals are with the following parameters **:**

-Type of signal: sinusoidal with (f_{START} = 0.5 MHz) and (f_{STOP} =2 MHz).

-Maximum frequency range of DDFS: (0.011 Hz…25 MHz).

-Frequency resolution of DDFS: (0.011 Hz).

-Size of DDFS ROM: (8 x 16384 bits=14KB).

-DAC: with (8) bits.

-Bits number of Phase Accumulator (PA): (n=32) bits.

Signal amplitude (5V).

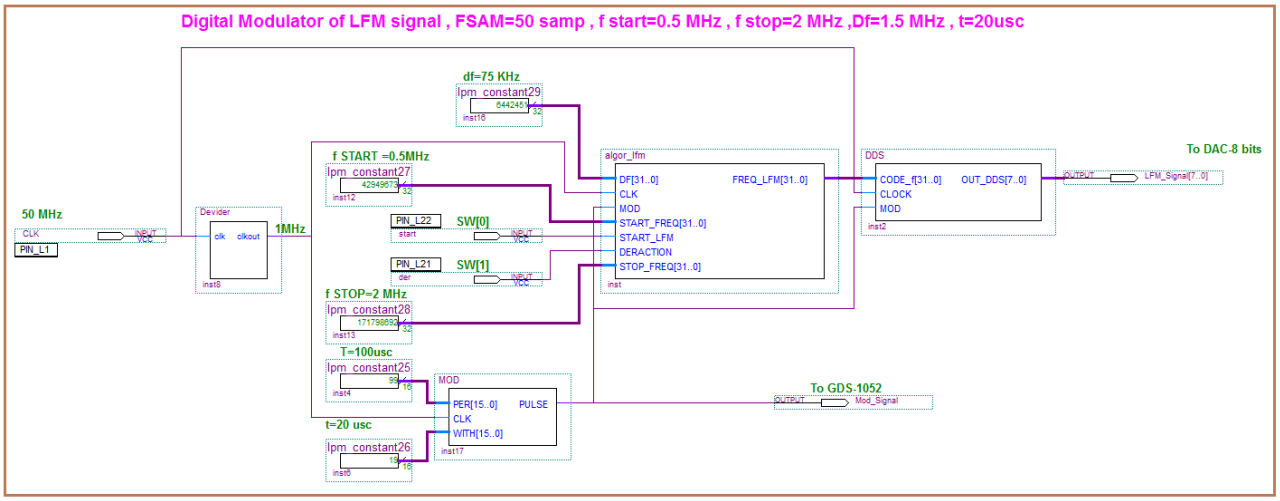

Fig. (8): The functional diagram of the digital LFM synthesizer using DDFS

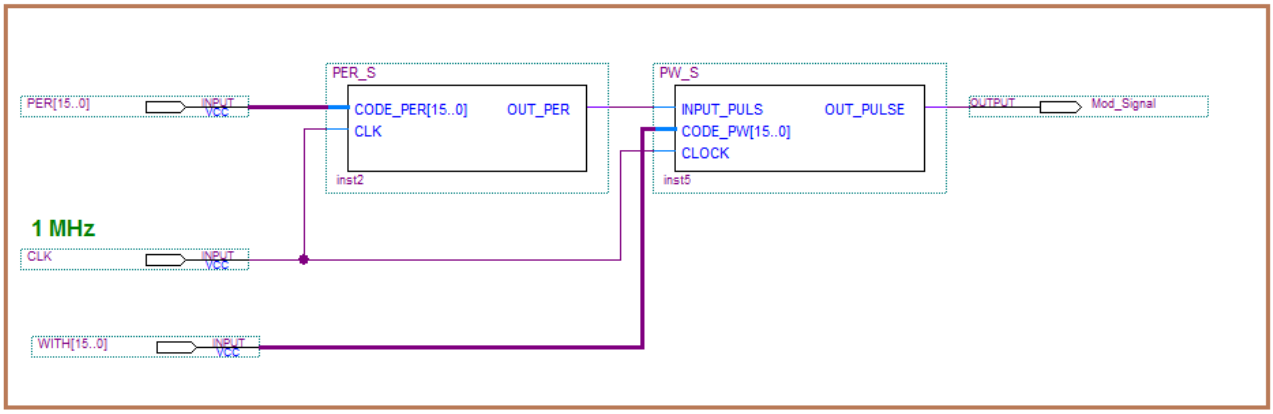

Fig. (9): The functional diagram of the digital pulse synthesizer (DPS)

International Multidisciplinary Research Journal Reviews (IMRJR)

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

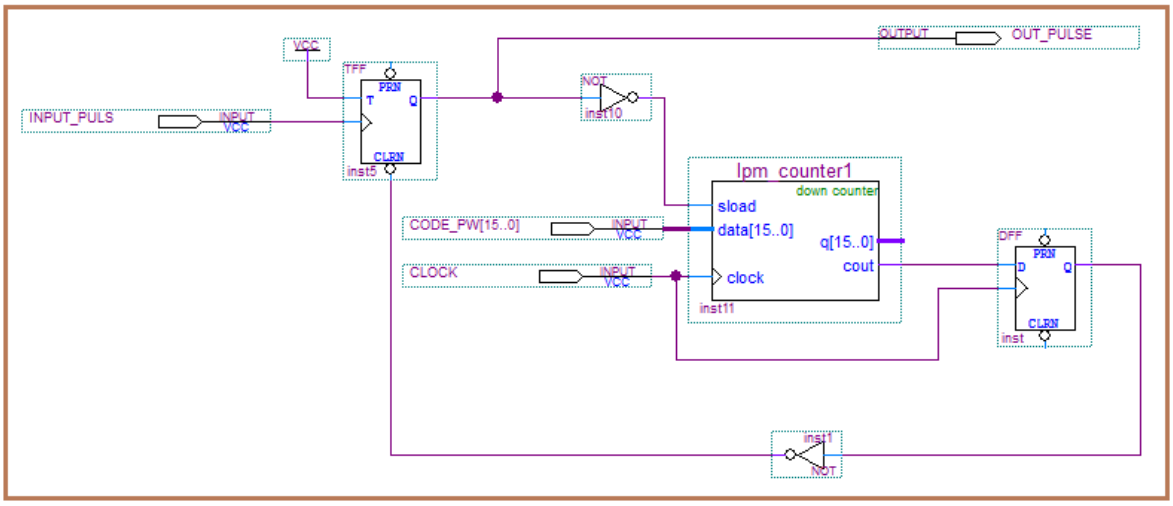

Fig. (10): The synthesizer of pulses width in DPS

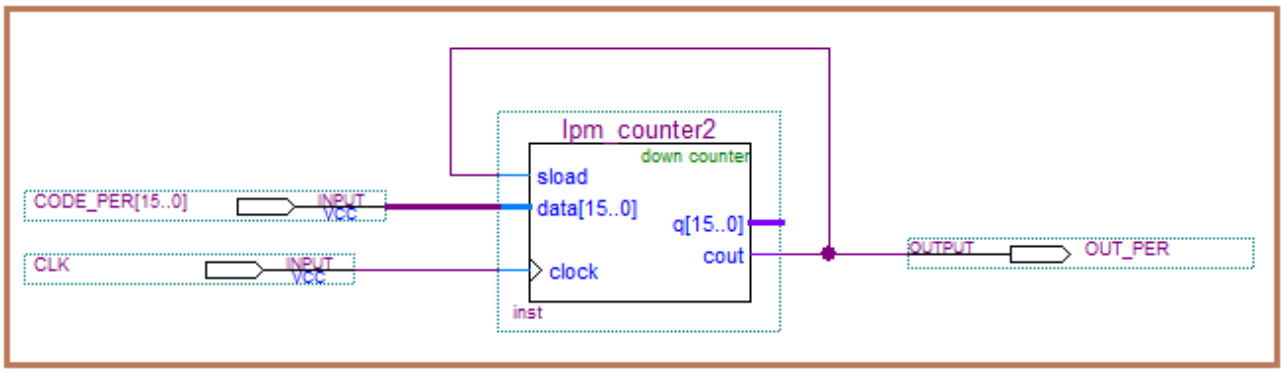

Fig. (11): The synthesizer of pulses period in DPS

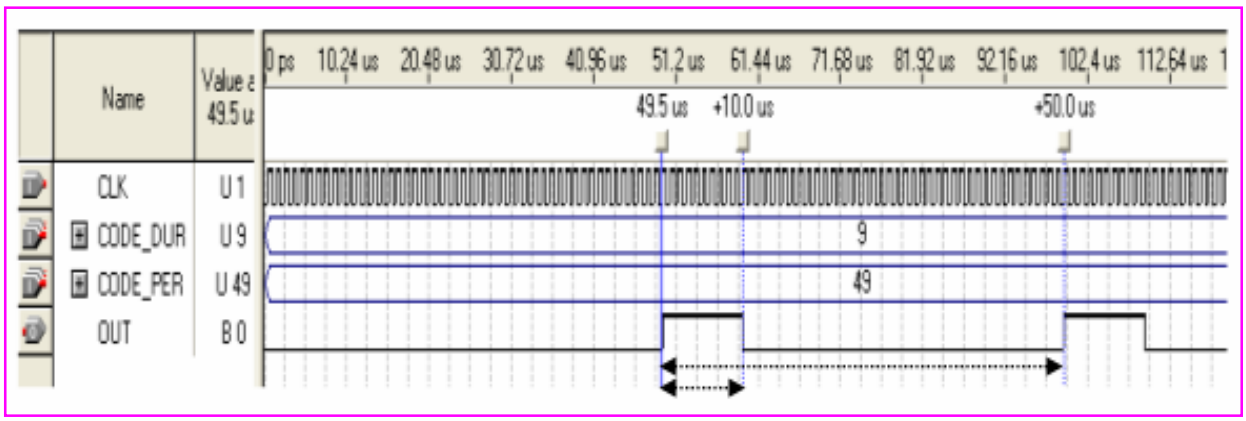

Fig. (12): The simulation signal of DPS in time domain

International Multidisciplinary Research Journal Reviews (IMRJR)

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

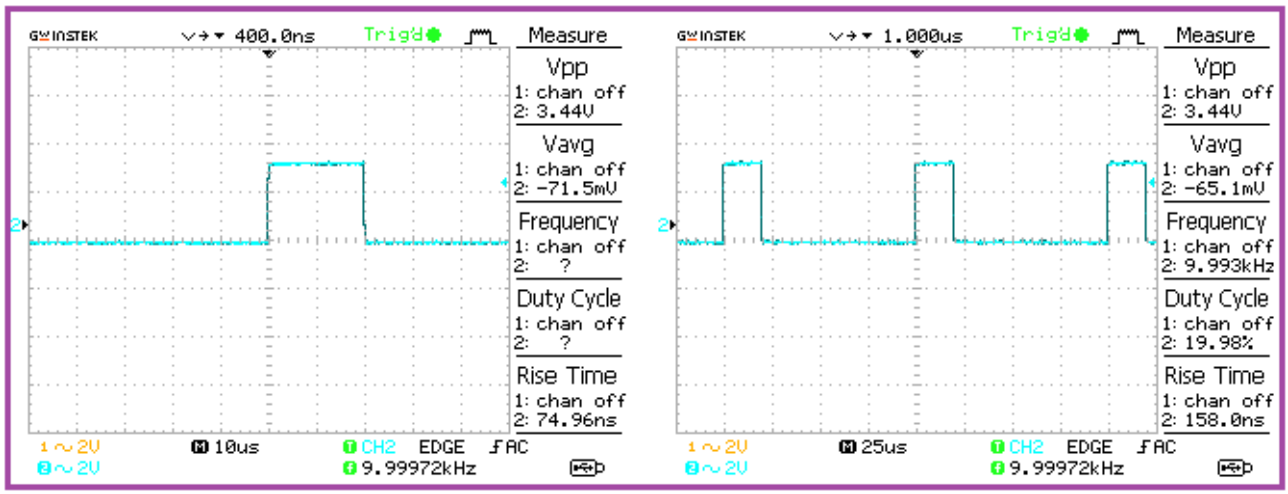

Fig. (13): The pulse signal of DPS in time domain $(\tau = 20\,\mu\,\text{sec}, \text{T} = 100\,\mu\,\text{SEC})$

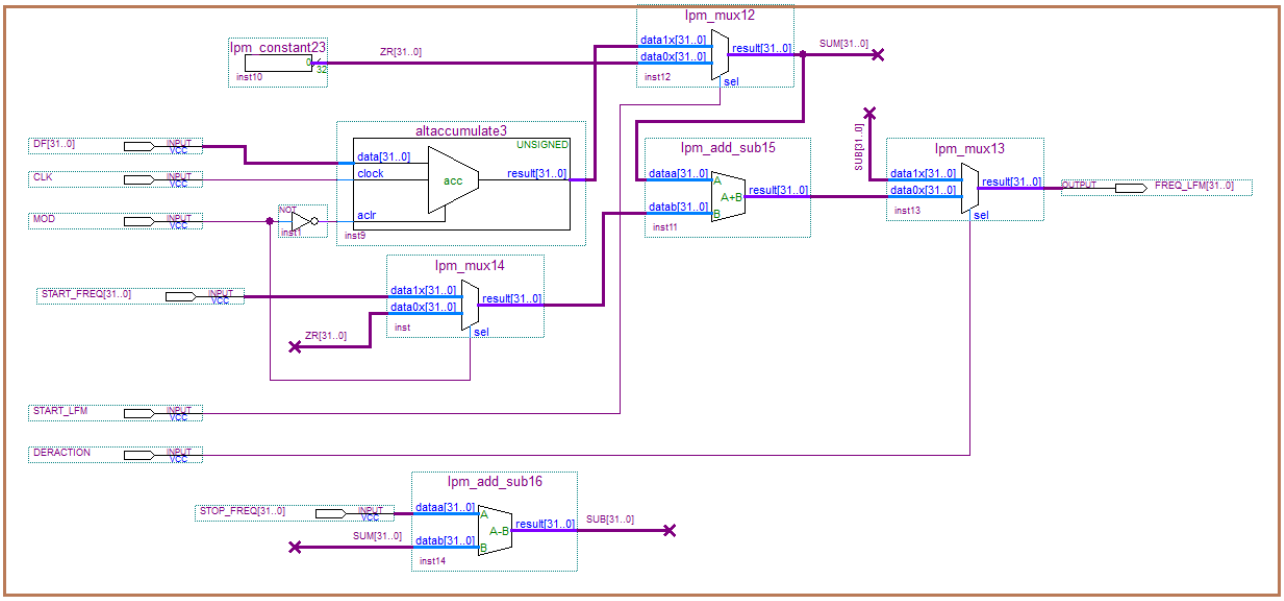

Fig. (14): The functional diagram of the LFM algorithm

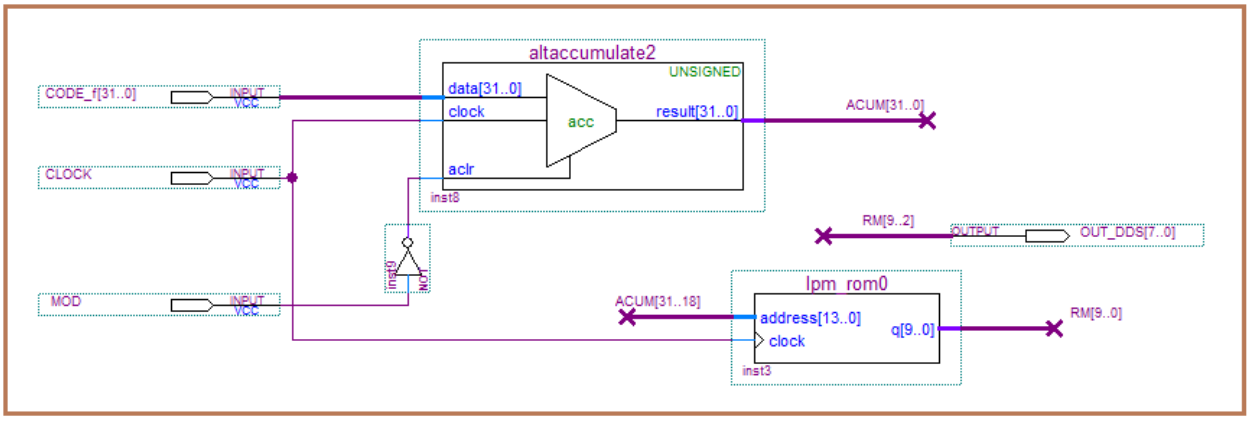

Fig. (15): The functional diagram of DDFS for LFM

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

The practical results of the LFM synthesizer in time domain according to the previous application are shown in figure (16) in cases of increased, decreased LFM, and without LFM. These figures are taken from a digital oscilloscope and spectrum analyzer of type GDS-1052U. We note the big (identification- similarity) between the theoretical results and the practical results, which indicates the high accuracy of digital synthesizing and modulation operations for signals.

Figure (17) show the spectrum of pulse modulation signal and the spectrum of LFM signal for:

$(\Delta f_1 = 0.5MHz\,, \Delta f_2 = 2\,MHz\ \ and\ \ \tau = 20\mu sec)$

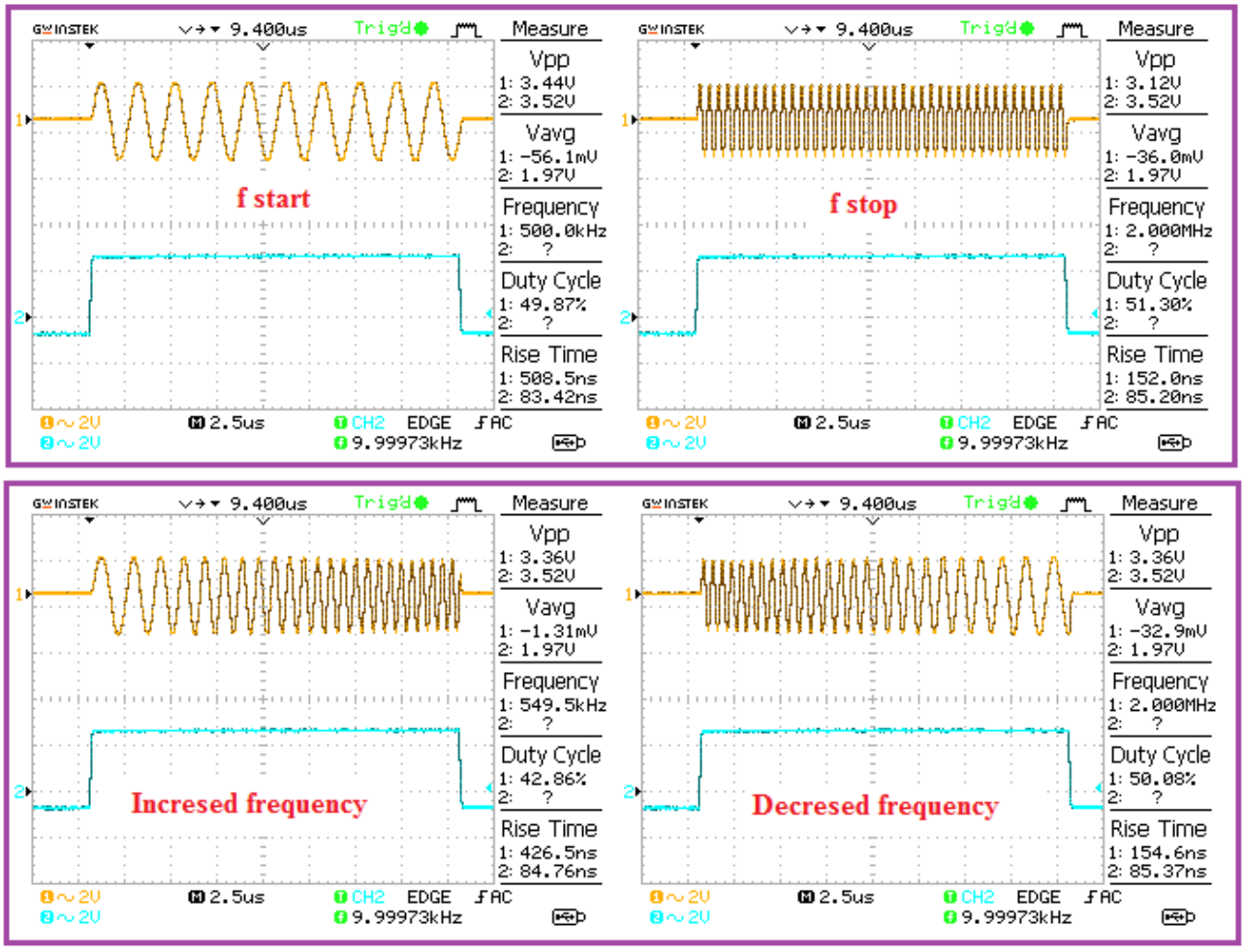

Fig (16) radio pulse and LFM signals (increased and decreased frequency) in time domain

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 4, December 2024
DOI 10.17148/IMRJR.2024.010402

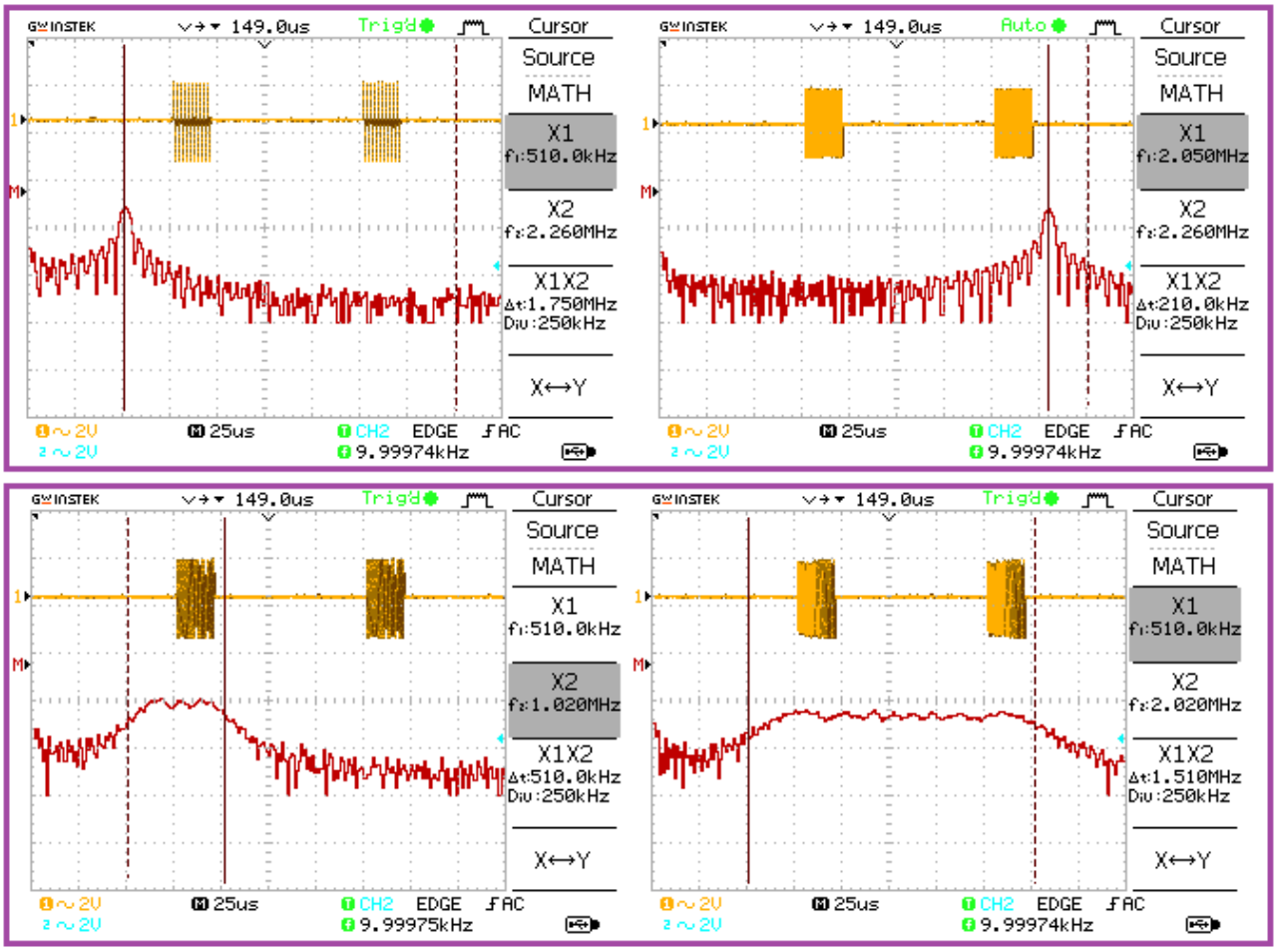

Fig (17) spectrum of pulse and LFM signals in frequency domain

VII. DISCUSSION AND CONCLUSION

-Using DDFS techniques in radar domain allows implementing different digital modulation operations (pulse, LFM, BPSK according to Barker codes, coherent and etc) with high accuracy and speed in digital signal synthesizing, and with the ability of changing parameters in wide range.
-Using DDFS techniques in radar domain allows implementing the digital processing in the radar receiver on high intermediate frequency.
-We note from the practical results the big identification-similarity between the theoretical results and the practical results, which indicates the high accuracy of digital synthesizing and modulation operations for signals.
-The designs can be developed and modified according to user requirements due to the use of reprogrammable chips (FPGA).
-The most important thing in this paper is the possibility of changing the frequency range within the pulse width due to large limits as well as changing the pulse width. This allows obtaining a spread spectrum signal with a very low spectral density, which increases the interference resistance of these signals, and thus increases the protection against jamming.

REFERENCES

[1] Fuqin Xiong, “digital Modulation Techniques”, Artech House telecommunications library, /653/ pages., 2000
[2] GOLDBERG B. 1999- Digital Frequency Synthesis Demystified, LLH Technology Publishing, united states, 334.
[3] April 2017 , DOI:10.1109/ICECA.2017.8212806 International conference of Electronics, Communication and Aerospace Technology (ICECA), Design and implementation of linear frequency modulated waveform using DDS and FPGA

[4] Raeshma. K.V M.Tech , Waveform Generation Based on Complete DDS Tech.for RADARs,International Journal of Engineering Research & Technology (IJERT) IJERT ISSN: 2278-0181 www.ijert. Vol. 3 Issue 7, July - 2014.
[5] ALTERA, CORPORATION," Cyclone II Device Family Data Sheet"; 2005.
[6] Volnei A. Pedroni, Circuit Design With VHDL, MIT Press Cambridge, Massa- chusetts London, England (2004) 364.
[7] Dr. Kamal Aboutabikh, Dr. Abdul-Aziz Shokyfeh, Dr. Amer Garib, "Design and Implementation of a Digital Quadrature Amplitude Modulator QAM-16 using FPGA", International Multidisciplinary Research Journal Reviews , Volume 1, Issue, 2, October 2024.
[8] Merrill I. SkolinK , RADAR HANDBOOK ,Third Edition ,New York Chicago San Francisco Lisbon London Madrid Mexico City Milan new Delhi san Juan Seoul Singapore Sydney Toronto.
[9] ANALOG DIVISE, A Technical Tutorial on Digital Signal Synthesis.

BIOGRAPHY

Dr. Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR , university of communication in Leningrad , holds a degree assistant professor in 2009 from Aleppo university.
Lecturer at Department of Biomedical Engineering , Al Andalus University For Medical Sciences-Syria ,Tishreen University-Syria ,Corduba Private University- Syria , Kassala University-Sudan and Ittihad Private University- Syria.
Publish a lot of research in the field of digital communication and digital signal processing in the universities journals of Syria and in the European and Indian journals.
Working in the field of programming FPGA by using VHDL and design of Digital Filters.

Dr. Abdul-Aziz Shokyfeh holds a PhD in telecom engineering in 2017 from Damascus Syria, Faculty of Mechanical and Electrical Engineering Telecommunication and electronic department .
Lecture at Electric engineering , computer engineering , control and automation engineering, telecom and electronic engineering at Damascus University.
Dean of IT college at Ittehad Private University, from 2023 till now.
Publish a lot of research in field of antenna in Syrian and European journals .Working in field of PBXs Network , low current system and solution.

Dr. Amer Garib holds a PhD in communication engineering in 1994 from the USSR, university of communication in Leningrad. Lecturer at Department of Faculty of Informatics Engineering , Ittihad Private University- Syria.
Publish a lot of research in the field of digital communication in the universities of Syria and in the Indian journals.
Working in the field of Digital Communication Systems and design of Antenna Systems.