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# Design And Implementation of Computer-Controlled Direct Sequence Spread Spectrum (DSSS) System Using FPGA

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**Abstract:** Spectrum spreading techniques is used in CDMA communications systems, where that each subscriber within the communication system is assigned one pseudo noise code.
The number of codes equal to the number of subscribers to the communications system.
In this paper, we discuss a practical mechanism design of the Direct Sequence Spread Spectrum (DSSS) system which is used in CDMA communication systems by using cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1 with the following parameters:
-Clock frequency :$F_{CLK}$=50MHz
-Modulation type of signal is: BPSK
-Frequency range is: (3Hz…..10 MHz ).
-Frequency Resolution is: (3Hz).
-Frequency of data impulses ($F_{DATA}$=1KHz).
-Frequency of pseudo-noise code generator (PNCG): ($F_{PNCG}$=50,100,500,1000 KHz).
-Spreading spectrum factor: $K_{SS}$= ($F_{PNCG}/F_{DATA}$ )=50,100,500,1000.
maximum length of PNCG for (10 bits) shift register is:$\{L_{PNCG} = (2^{10} - 1) * T_{PNCG}\}$
-Signal amplitude (5V).
-Computer-controlled parameters: operating frequency, Spreading spectrum factor value.
-Possibility of updating: Increasing the spreading spectrum factor, Increasing the number of bits of the pseudo-random sequence generator so that the spectrum becomes more random, change modulation type, increase the frequency range up to 20 MHz

**Keywords:** DSSS, CDMA, BPSK, FPGA, PNCG, DDFS, DDS, Spread spectrum.

## I. INTRODUCTION

The mathematical principle of spreading the spectrum using DSSS can be explained according to the diagram shown in figure 1, where the spectrum of the data signal is spread according to a PNCG and a mathematical spreading function at the transmitting side.
While on the receiving side, the process is the opposite, so that the spectrum is collected according to the same PNCG and the mathematical spreading function to obtain the initial spectrum of the data signal.
In paper [1], the DSSS is designed for pseudo-noise code generator with only (11) chips, while in this research we have 1000 clips and it is possible to develop up to 5000 clips.
In paper [2] , the DSSS is designed for pseudo-noise code generator with only (10….128) chips, where pseudo noise code generator it is generated 127 bit gold sequence which is used for spreading , while in this research we have 1000 clips and it is possible to develop up to 5000 clips and the phase resolution $0.044^{o}$ while in this research we have $0.44^{0}$ .

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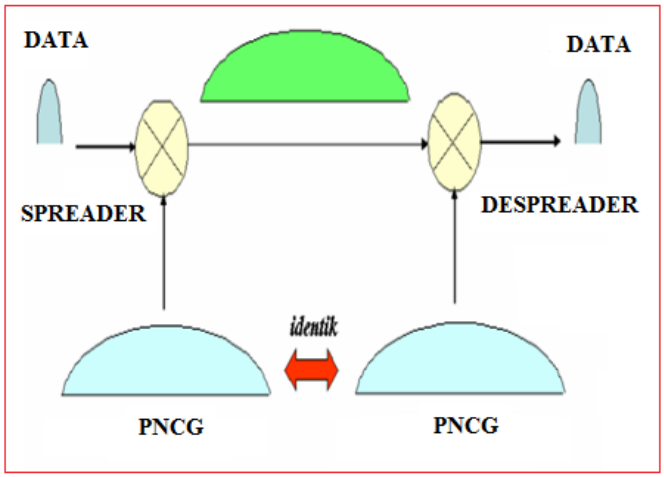


Figure (1) principle of spreading the spectrum using DSSS

## II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

-Using the digital DDFS with digital BPSK modulation, digital square generator of data, digital impulse generator of spreading spectrum factor and pseudo-noise code generator, it makes the DSSS design process flexible, accurate and highly efficient.

-Changing the spreading spectrum factor within different values explains the difference between DSSS systems, this factor determines the number of subscribers to the communications system and thus the effectiveness of this system.

## III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the DSSS for different spreading spectrum factor of signals, the following tools and software are used:
-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [3].
-DDFS which is considered as highly accuracy techniques in sinusoidal and squares signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment [4].
-Design Environment MATLAB R2008a
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the chip of FPGA .
The block diagram of the laboratory experiment platform is shown in figure (2).

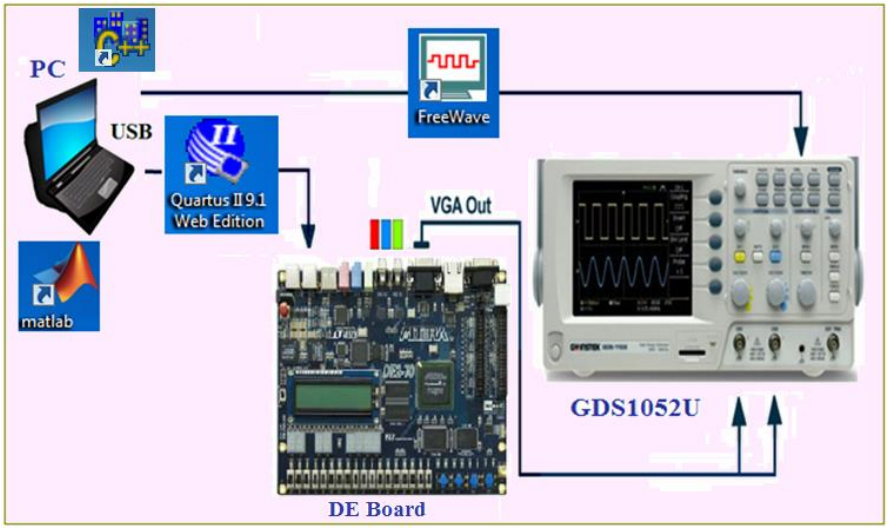


Figure (2) Block diagram connection of the laboratory experiment platform

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## IV. BLOCK DIAGRAM OF A DSSS

The block diagram of the DSSS is shown in figure (3) and is composed of:
-Clock generator with: $F_{CLK}$=50 MHz.
-A first frequency divider with a division factor ($N_0$) to obtain the frequency of the data signal (DATA) from clock generator.
-A second frequency divider with a division factor {N(N1 ,N2, N3 ,N4)} to obtain the frequency of pseudo-noise code generator (PNCG) from clock generator.
-XOR gate to convert a bit of data into a pseudo-noise code.
-BPSK modulator.
-DDFS to shape the carrier signal for the BPSK.
So that the number of chips is always correct, there must be synchronization between the data pulses and the semi-random digital sequence, or the ratio between the data frequency and the clock frequency of the semi-random sequence generator must always be an integer.

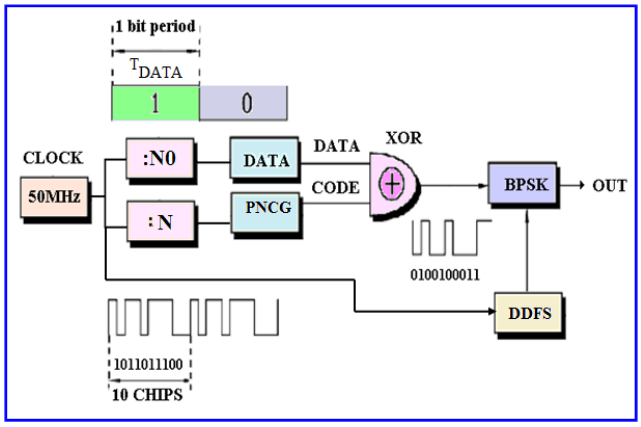


Figure (3) The block diagram of DSSS

Spreading the spectrum using DSSS depends on converting each data pulse (bit) into a set of short pulses ($T_c$) (a pseudo-noise code consisting of 1 and 0, each of which is called a segment or chip) according to the time diagram shown in figure (4) using the XOR function.

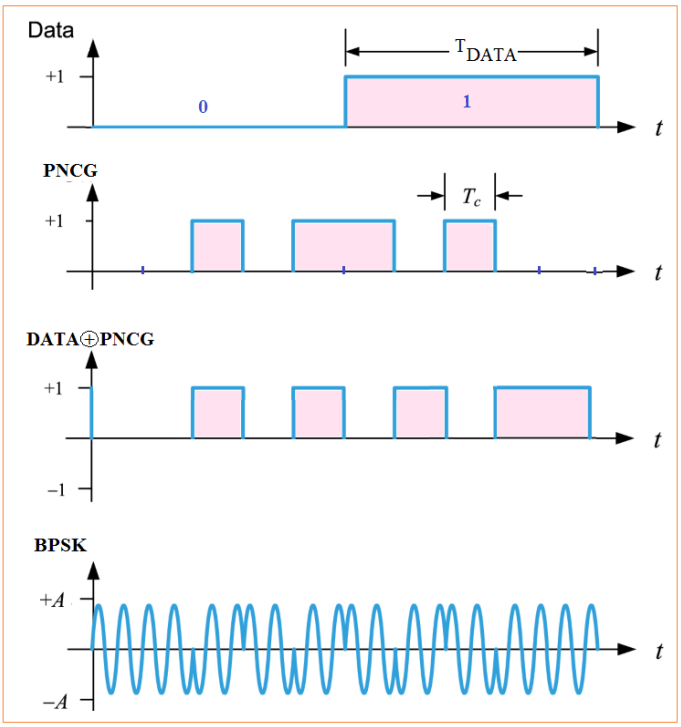


Figure (4) The signals of DSSS with BPSK in time domain

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## V. FUNCTIONAL DIAGRAM OF A SPECTRUM SPREADER DSSS

The block diagram of the DSSS is shown in figure (5) and is composed of:
-Frequency of the data signal generator (DATA) is calculate according following relation [5]:

$$F_{DATA} = 2 * \frac{F_{CLK}}{N_0} \qquad (1)$$

Where:

$$F_{DATA} = 2 * \frac{F_{CLK}}{N_0} = 2 * \frac{50 * 10^3}{100000} = 1 \text{ KHz}$$

-Frequency of the pseudo-noise code generator (PNCG) is calculate according following relation [5]:

$$F_{PNCG} = \frac{F_{CLK}}{N} \qquad (2)$$

Where:

$$F_{PNCG\_1} = \frac{F_{CLK}}{N_1} = \frac{50 * 10^3}{1000} = 50 \text{ KHz} \Rightarrow K_{SS\_1} = \frac{F_{PNCG\_1}}{F_{DATA}} = \frac{50}{1} = 50$$

$$F_{PNCG\_2} = \frac{F_{CLK}}{N_2} = \frac{50 * 10^3}{500} = 100 \text{ KHz} \Rightarrow K_{SS\_2} = \frac{F_{PNCG\_2}}{F_{DATA}} = \frac{100}{1} = 100$$

$$F_{PNCG\_3} = \frac{F_{CLK}}{N_3} = \frac{50 * 10^3}{100} = 500 \text{ KHz} \Rightarrow K_{SS\_3} = \frac{F_{PNCG\_3}}{F_{DATA}} = \frac{500}{1} = 500$$

$$F_{PNCG\_4} = \frac{F_{CLK}}{N_4} = \frac{50 * 10^3}{50} = 1000 \text{ KHz} \Rightarrow K_{SS\_4} = \frac{F_{PNCG\_3}}{F_{DATA}} = \frac{1000}{1} = 1000$$

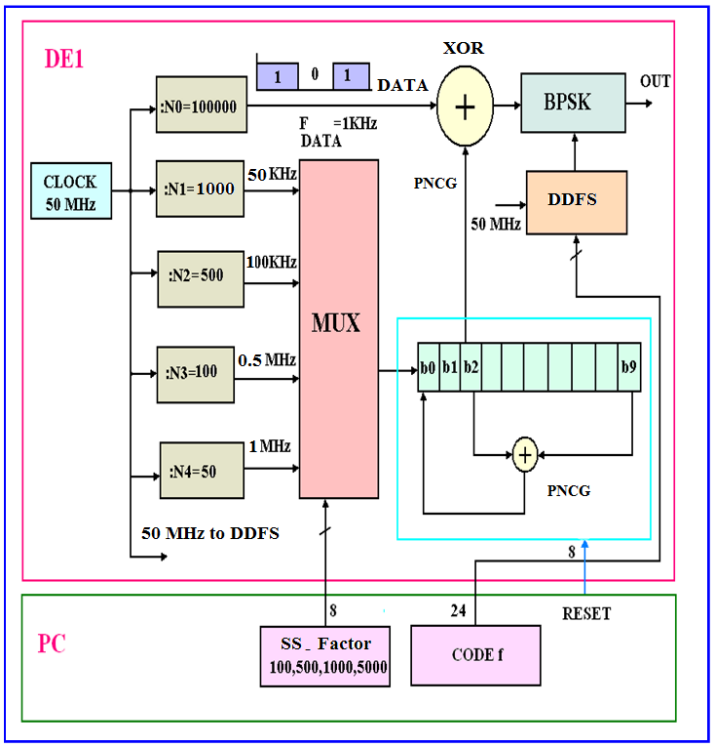


Figure (5) The functional diagram of a spectrum spreader DSSS

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The pseudo-noise code generator is a (k=10-bits) shift register with a non-zero initial state and a feedback connection as shown in the figure (6) in Quartus II 9.1 design environment [5].
It must be remembered that the method of feedback connection in the shift register and its initial state determine the role of code repetition, which is specific to each subscriber within a single communication system.
This feedback of the shift register achieves the maximum period or length of the code [5]:

$$L_{PNCG} = (2^k\text{-}1)*\mathrm{T}_{\mathrm{PNCG}} \qquad (3)$$

$$T_{PNCG\_1} = 1/F_{PNCG\_1} = \frac{1}{50} = 0.02 \text{ msec} \Rightarrow \mathrm{L}_{\mathrm{PNCG\_1}} = (2^{10}-1) * 0.02 = 20.46 \text{ msec}$$

$$T_{PNCG\_2} = 1/F_{PNCG\_2} = \frac{1}{100} = 0.01 \text{ msec} \Rightarrow \mathrm{L}_{\mathrm{PNCG\_2}} = (2^{10}-1) * 0.01 = 10.23 \text{ msec}$$

$$T_{PNCG\_3} = 1/F_{PNCG\_3} = \frac{1}{500} = 0.002 \text{ msec} \Rightarrow \mathrm{L}_{\mathrm{PNCG\_3}} = (2^{10}-1) * 0.01 = 2.046 \text{ msec}$$

$$T_{PNCG\_4} = 1/F_{PNCG\_4} = \frac{1}{100} = 0.001 \text{ msec} \Rightarrow \mathrm{L}_{\mathrm{PNCG\_4}} = (2^{10}-1) * 0.001 = 0.2046 \text{ msec}$$

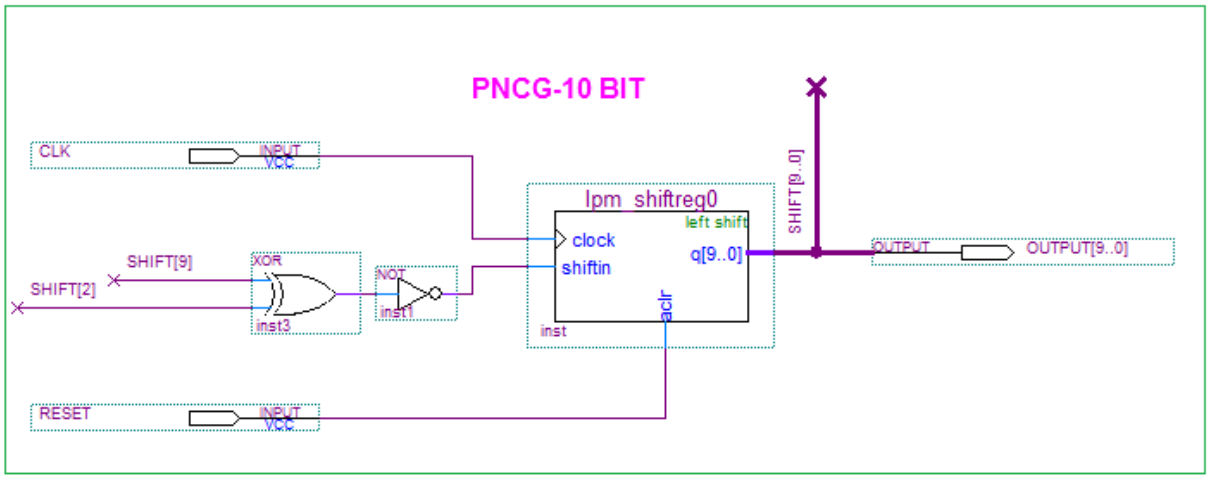


Figure (6) Functional diagram of a PNCG in Quartus II 9.1 design environment

## VI. BLOCK AND FUNCTIONAL DIAGRAM OF A BPSK MODULATOR

The block diagram of the BPSK modulator is shown in figure (7) [4], and the functional diagram of the BPSK modulator is shown in figure (8) [6].

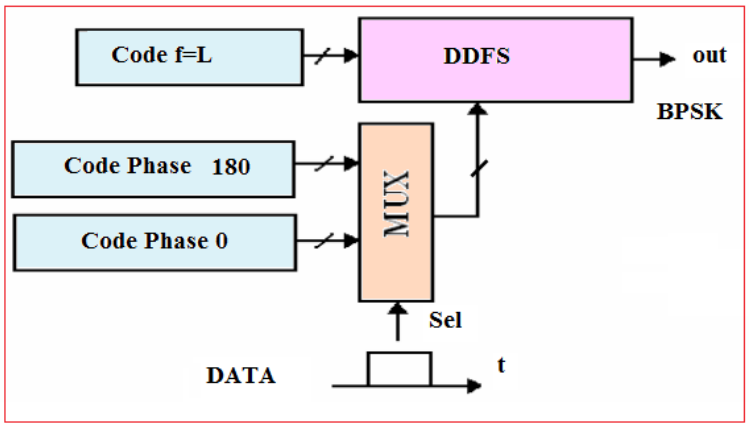


Figure (7) The block diagram of the BPSK modulator

- Operating frequency of the DDFS is calculate according the following relation [7]:

Frequency Resolution is:

$$\delta f = \frac{F_{CLK}}{2^n} = \frac{50*10^6}{2^{24}} = 3 \text{ Hz}$$

Phase Resolution is:

$$\delta\phi = \frac{360}{2^b} = \frac{360}{2^{13}} = 0.044^0$$

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$$F_{OUT} = \frac{F_{CLK} * L}{2^n} \qquad (4)$$

Where:

$$L = \frac{2^n . F_{OUT}}{F_{CLK}} \qquad (5)$$

For: n=24 bits and $F_{OUT}$=1 MHz to:

$$L = \frac{2^n . F_{OUT}}{F_{CLK}} = \frac{2^{24} * 1}{50} = 335544$$

- Code of phase of BPSK modulation is calculate according following relation [5]:

$$CODE\ \text{PHASE}\ = X_{\phi} = \frac{2^n . \phi}{2\pi} \qquad (6)$$

For : n=24 bits and $\phi = 0$ rad to:

$$CODE\ \text{PHASE} = \ X_{\phi=0} = \frac{2^n . 0}{2\pi} = 0$$

For : n=24 bits and $\phi = \pi$ rad to:

$$CODE\ \text{PHASE}\ = X_{\phi=\pi}\ = \frac{2^n . \pi}{2\pi} = \frac{2^{24}}{2} = 8388608$$

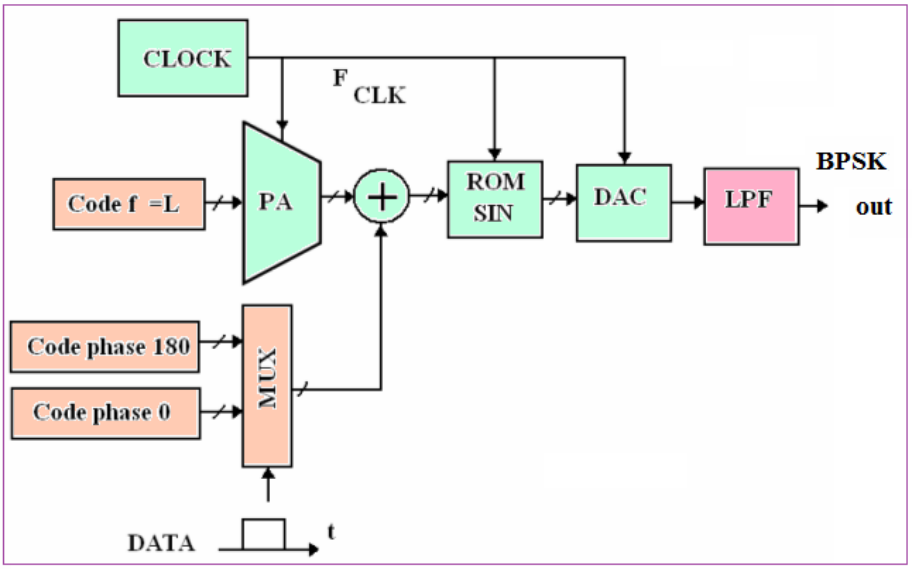


Figure (8) The functional diagram of the BPSK modulator

The functional diagram of the DDFS-BPSK modulator in Quartus II 9.1 design environment is shown in figure (9) [7] .

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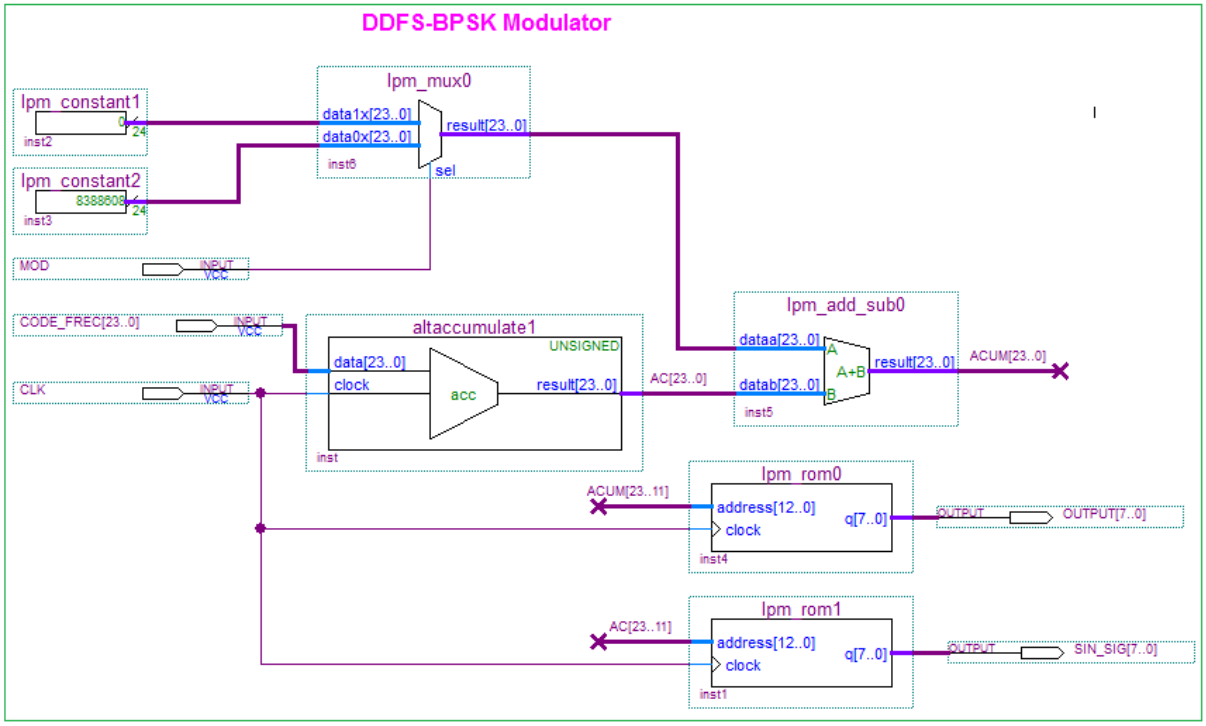


Figure (9) The functional diagram of BPSK modulator in Quartus II 9.1 design environment

The results of the practical design of a DDFS-BPSK modulator in time domain for ($K_{SS}$=50) and operating frequency ($F_{OUT}$ = 50 KHz) is shown in figure (10).

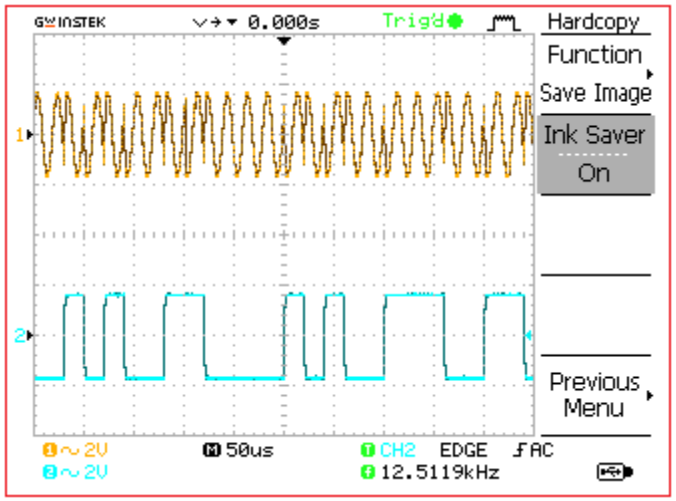


Figure (10) The output signal of DDFS-BPSK modulator in time domain

The functional diagram of PNCG and data generators DSSS system in Quartus II 9.1 design environment is shown in figure (11) [8]

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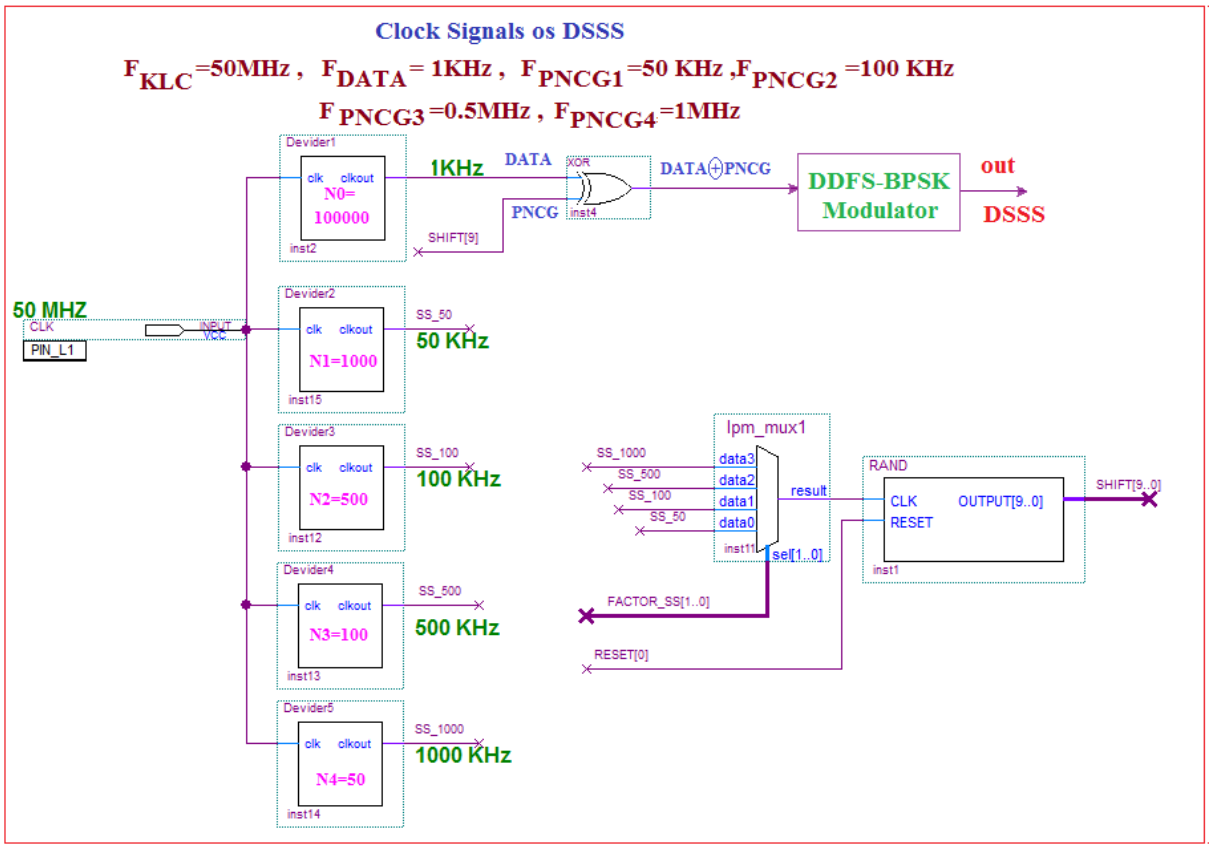


Figure (11) functional diagram of the clock signals of DSSS in Quartus II 9.1 design environment

## VII. PC INTERFACE OF CONTROLLING THE DSSS LABORATORY EXPERIMENT PLATFORM

This interface is shown in figure (12) and is designed within the programming environment (C++ BILDOR 6) and allows opening and closing the connection with the computer through the USB port and sending (7X8 bit) data in serial form from the computer to the development board DE-1. The sent data includes: 3Byte for the frequency code, 1Byte to choose the spreading spectrum factor ($K_{SS}$= 50,100,500,1000), 1Byte to reset the DSSS laboratory experiment, 2Byte for controlling and synchronization purposes.

Controls through the interface:

- Entering the desired frequency value in units of hertz (Hz).
- Choose the deployment factor 100,500,1000,5000.
- Executing or canceling the publishing process.
- Open the USB port using the (OPEN_USB) button.
- Send data to the board using the (SEND) button.
- Close the USB port using the (CLOSE_USB) button.
- Close the control program using the CLOSE button.

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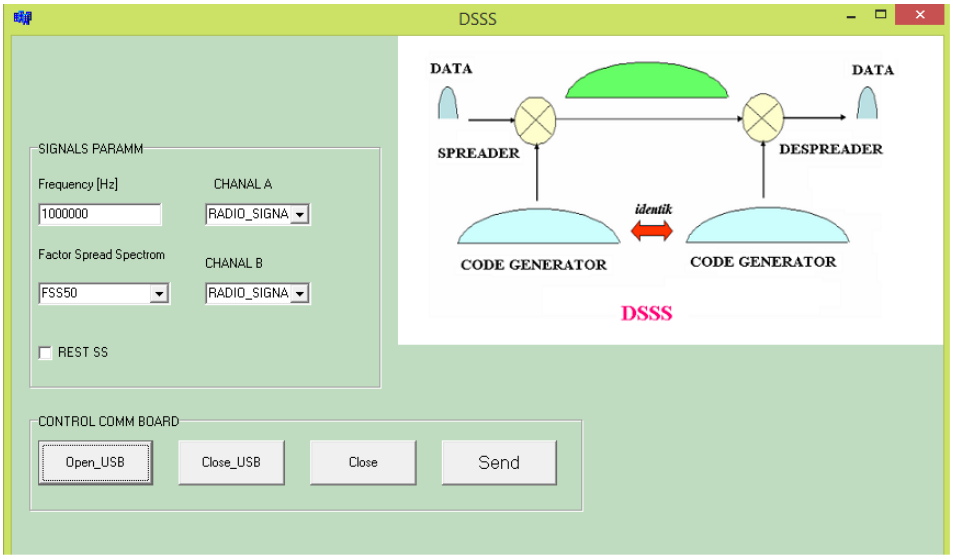


Figure (12) The interface of controlling the laboratory experiment platform

## XIII. CONCLUSION AND RESULTS

-The results of the practical design of a digital DSSS in time domain for different values of spreading spectrum factor ($K_{SS}$=50 ,100,500 ,1000) is shown in figure (13).
-The results of the practical design of a digital DSSS in frequency domain for different values of spreading spectrum factor ($K_{SS}$=50 ,100,500 ,1000) is shown in figure (14).
-By increasing the spread spectrum factor ($K_{SS}$), the band width of the spectrum of the spread signal increases until it approaches noise level (as shown in figure (14)), and the number of chips within a data bit increases (as shown in figure (13)), and thus the capacity of the communications system increases.
-The most importance in this paper is the possibility of changing the spreading spectrum factor ($K_{SS}$) within a large range of up to 5000.

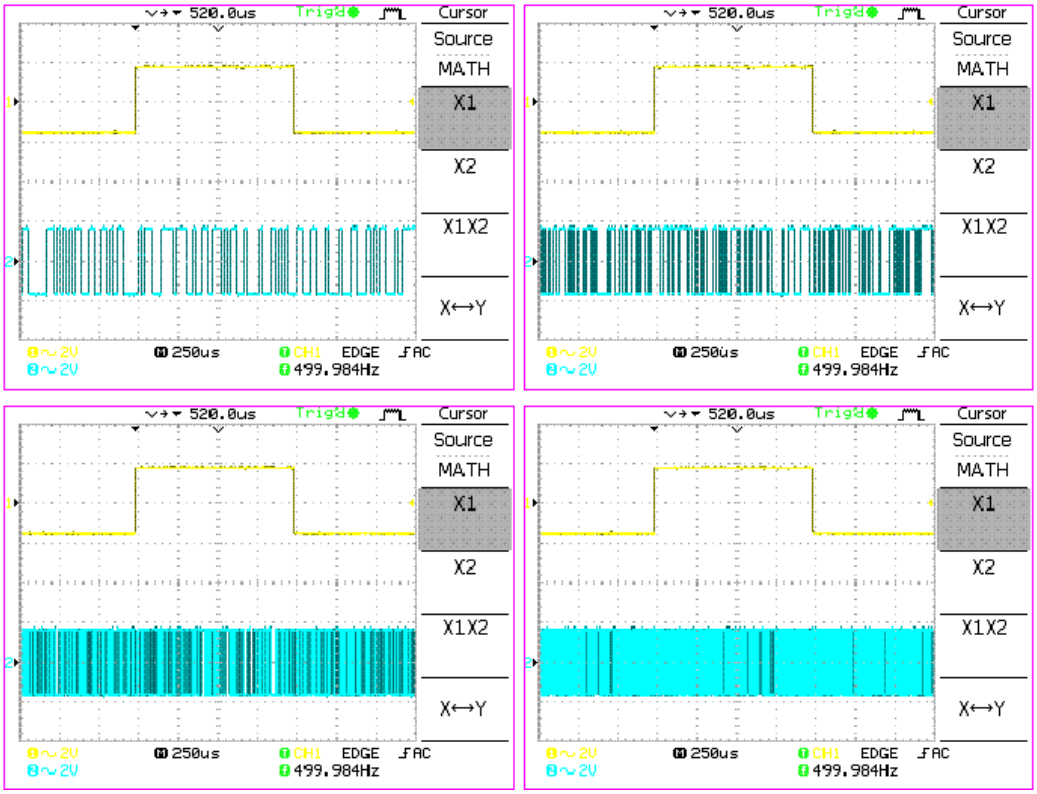


Figure (13) The results in time domain of practical design of DSSS for DATA and PNCG signals for $K_{SS}$=50 , 100 ,500 ,1000

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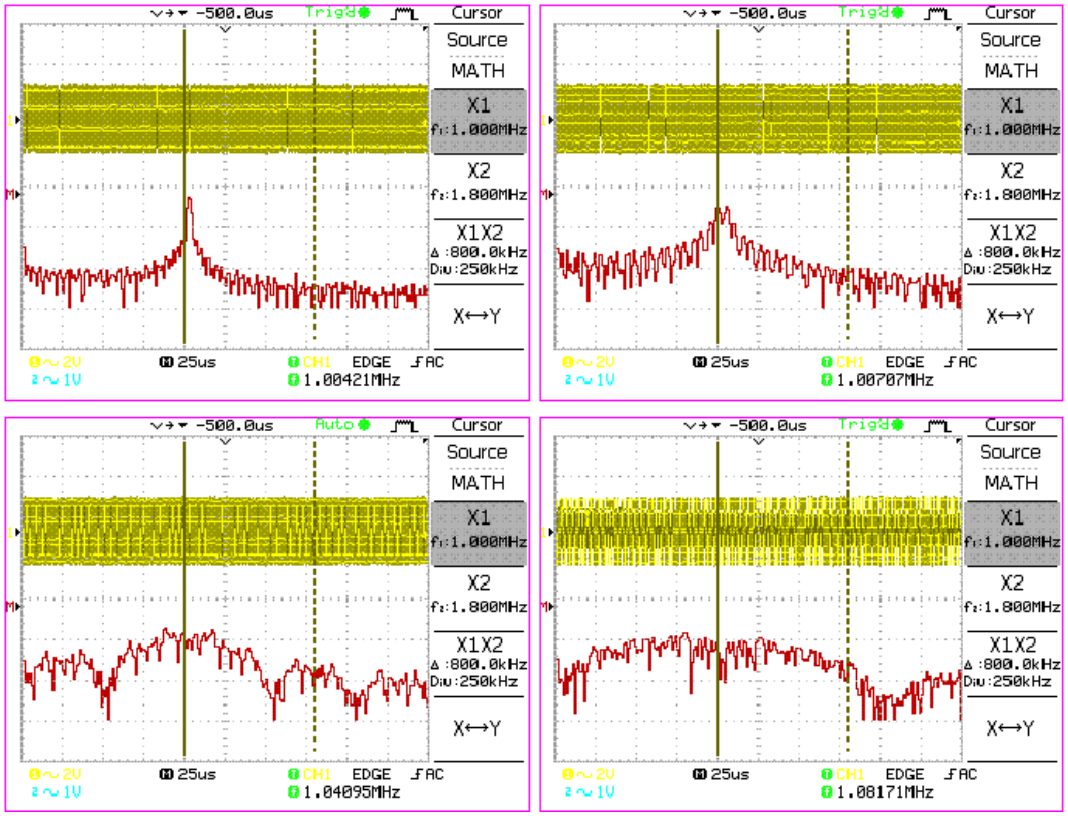


Figure (14) The results in frequency domain of practical design of DSSS for BPSK signals after modulation for $K_{SS}$=50 , 100 ,500 ,1000

## REFERENCES

[1]. Hamsa A. ABDULLAH , Raya K. MOHAMMED, DSSS-DRMC BASED SECURE TRANSMISSION WITH FPGA IMPLEMENTATION ,U.P.B. Sci. Bull., Series C,Vol. 83, Issue 1, 2021 ISSN 2286-3540.
[2]. R. Sarojini, Ch.Rambabu , Design and Implementation of DSSS-CDMA Transmitter and Receiver for Reconfigurable Links Using FPGA, International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-1, Issue-3, August 2012.
[3]. www.altera.com.
[4]. Volnei A. Pedroni, Circuit Design With VHDL, MIT Press Cambridge, Massa- chusetts London, England (2004) 364.
[5]. Afaq Ahmad, Sayyid Samir Al-Busaidi and Mufeed Juma Al-Musharafi .On Properties of PN Sequences Generated by LFSR – a Generalized Study and Simulation Modeling. Indian Journal of Science and Technology-2013.
[6]. GOLDBERG B. 1999- Digital Frequency Synthesis Demystified, LLH Technology Publishing, united states, 334.
[7]. Dr. Kamal Aboutabikh, Dr. Ibrahim Haidar , Digital compressing of a BPCM signal according to Barker code using FPGA , International Journal of Technical Research and Applications e-ISSN: 2320-8163, www.ijtra.com Volume 3, Issue 4 (July-August 2015), PP. 73-79.
[8]. Hemanth Kumar S N , Venkateshappa , Design and Implementation of DDS Module on FPGA, International Journal of Advanced Trends in Computer Science and Engineering , Volume 10, No.2, March - April 2021.

## BIOGRAPHY

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