

Design and Implementation of a Digital Quadrature Amplitude Modulator QAM-64 using FPGA

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Abstract: In this paper, we propose the design and implementation mechanism for different digital modulators such as Quadrature Amplitude QAM-64 modulators based on the use of Quadrature Direct Digital Frequency Synthesizer (QDDFS) using Cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1 with the following parameters:

- Clock frequency : $F_{CLK}=50\text{MHz}$.
- Modulation type of signal is : QAM-64 .
- Frequency range : (0.011 Hz...10 MHz) .
- Frequency Resolution : (0.011 Hz) .
- Signal amplitude(5V) .
- Data frequency : 1KHz .
- Digital designs allow the slides to modify and design development for results and better through reprogramming, depending on the user's desire.

Keywords : Digital Modulator ,QAM , QAM-46 , DDFS, QDDFS , FPGA.

I. INTRODUCTION

The mathematical principle of digital QAM modulation using QDDFS can be explained according to the diagram [1] shown in figure (1), where the Quadrature Amplitude Modulation achieved on multiply of data signal and samples of sinusoidal and cosine signals [2] stored in ROMs of QDDFS .

QAM-64 modulation achieved on adding (I. $\cos w_c t$) and (Q. $\sin w_c t$) signals from the QDDFS , where:

$$I = \pm 1 , \pm 3 , \pm 5 , \pm 7 , \quad Q = \pm 1 , \pm 3 , \pm 5 , \pm 7 \quad (1)$$

The stored values of the sine and cosine signals in ROM of DDFS and QDDFS are calculated according to the following equation [3]:

$$U_{SIN}(i) = INT \left[(2^{m-1} - 1) \cdot \sin \left(\frac{360 \cdot i}{2^b} \right) \right] \quad (2)$$

$$U_{COS}(i) = INT \left[(2^{m-1} - 1) \cdot \cos \left(\frac{360 \cdot i}{2^b} \right) \right]$$

For:

$$m = 8 \text{ bits} , b = 13 \text{ bits} , i = (0 \dots 2^b - 1) = (0 \dots 8191)$$

Then:

$$U_{SIN}(i) = INT \left[(2^{8-1} - 1) \cdot \sin \left(\frac{360 \cdot i}{2^{13}} \right) \right] = INT \left[127 \cdot \sin \left(\frac{360 \cdot i}{8192} \right) \right]$$

$$U_{COS}(i) = INT \left[(2^{8-1} - 1) \cdot \cos \left(\frac{360 \cdot i}{2^{13}} \right) \right] = INT \left[127 \cdot \cos \left(\frac{360 \cdot i}{8192} \right) \right]$$

$$U_{\sin}(i) = (-127..... + 127)$$

$$U_{\cos}(i) = (-127..... + 127)$$

To avoid negative values that are difficult to store in memory, we add a value off-set= 128

$$U_{\sin}(i) = (0.....255)$$

$$U_{\cos}(i) = (0.....255)$$

In paper [4] present the design and simulation only of a modulation module for ASK using VHDL.

In paper [5] present the design and simulation of a modulation module for ASK ,FSK,BPSK,QPSK using VHDL.

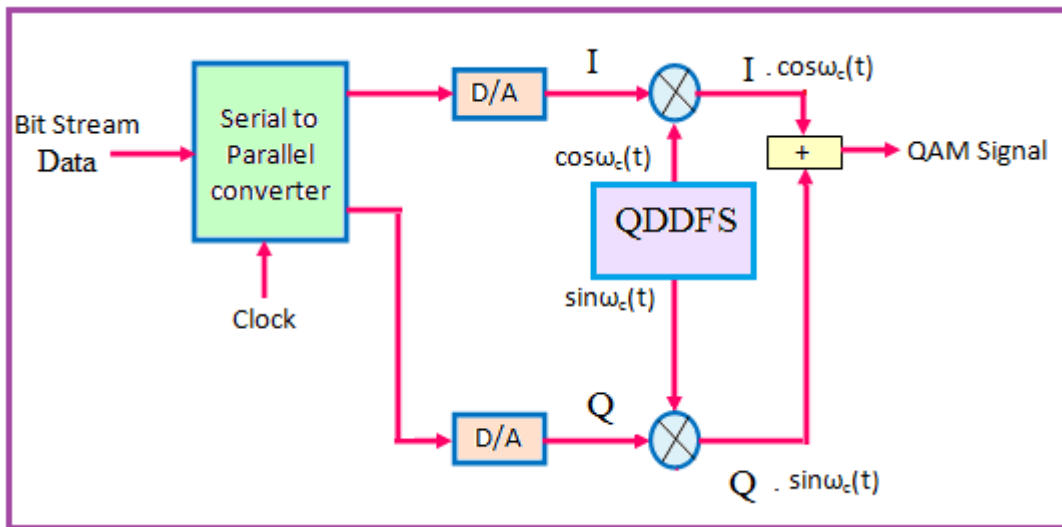


Figure (1) Block diagram of digital QAM modulator using QDDFS

II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

-In this paper digital QAM-64 modulator were designed, implemented and tested based on the use of Quadrature Digital Direct Frequency Synthesizer (QDDFS) using FPGA, VHDL and Graphical programming language with Quartus II 9.1 design environment.

-Using the digital QDDFS with mathematical operations (adding , multiply , division) , makes the digital modulation design process flexible, accurate and highly efficient.

-Changing the data signal frequency , carrier signal frequency, frequency deviation and phase shift within different values explains the difference between digital modulation and analog modulation .

III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the digital modulators for different modulation types of signals, the following tools and software are used:

-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [6].

-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.

-VHDL programming language with Quartus II 9.1 design environment [7].

-Design Environment MATLAB R2008a

-GDS-1052 digital oscilloscope with Free Wave program to take the results.

-PC computer for designing and injecting the design in the FPGA chip.

The block diagram of the laboratory experiment platform [8] is shown in figure (2).

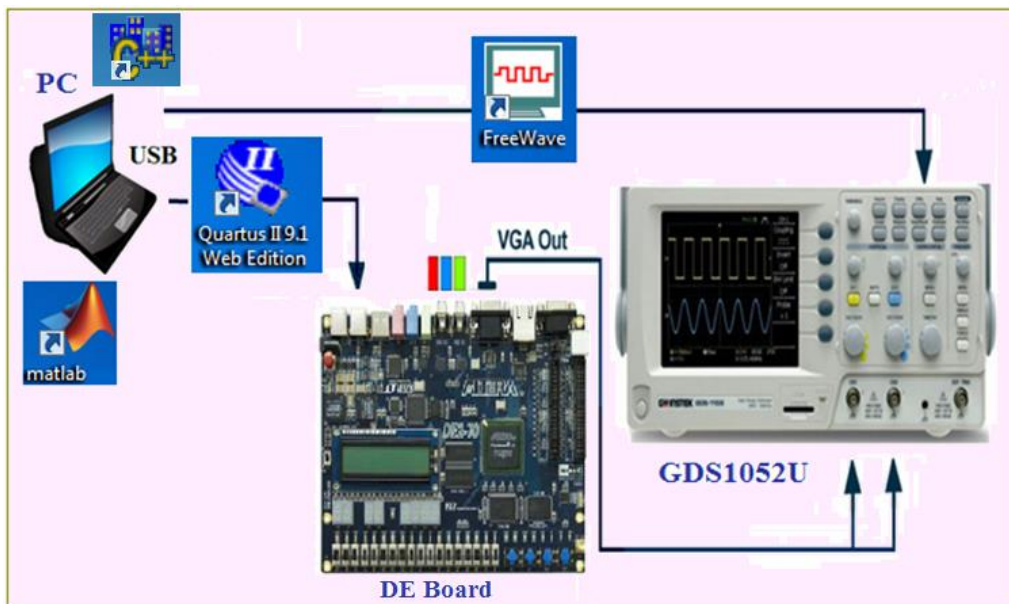


Figure (2) Block diagram of the laboratory experiment platform

IV. BLOCK AND FUNCTIONAL DIAGRAMS OF A DIGITAL QAM-64

The characteristics of QAM types is shown in table 1:

Table.1 : types of QAM		
Name of scheme	Bit per symbol (bits)	Number of symbols
QAM-4	2	$2^2=4$
QAM-8	3	$2^3=8$
QAM-16	4	$2^4=16$
QAM-32	5	$2^5=32$
QAM-64	6	$2^6=64$

The QAM-64 signal is given according to the following equation [3] :

$$U_{QAM-64}(t) = I \cdot \cos(2\pi f_c t) + Q \cdot \sin(2\pi f_c t) \quad (3)$$

$$U_{QAM-64}(t) = A \cdot \sin(2\pi f_c t + \theta)$$

Where:

$$\text{Amplitude} = A = \sqrt{(I)^2 + (Q)^2} = \sqrt{I^2 + Q^2} \quad (4)$$

$$\text{Phase} = \theta = \tan^{-1}\left(\frac{Q}{I}\right) \quad (5)$$

Where: $I = \pm 1, \pm 3, \pm 5, \pm 7$, $Q = \pm 1, \pm 3, \pm 5, \pm 7$, (w_c) carrier frequency of signal.

Values of Data (000000, ,111111), I component, Q component, QAM-64 output signal, amplitude and phase QAM-64 given according to the table .2, the constellation diagrams of QAM-64 signal shown in figure (3).

Table .2 values of : I, Q, QAM-64, Phase, Amplitude QAM-64 and scale factor									
N	Data	I	Q	I*cos	Q*sin	Out	Phase	Amplitude	Scale factor
0	000000	-7	-7	-7 cos	-7 sin	-7 cos-7sin	225	9.9	10
1	000001	-7	-5	-7 cos	-5 sin	-7 cos-5sin	216	8.6	9
2	000010	-7	-3	-7 cos	-3 sin	-7 cos-3sin	203	7.6	8
3	000011	-7	-1	-7 cos	-1 sin	-7 cos-sin	188	7.1	8

4	000100	-7	7	-7 cos	7 sin	-7 cos+7sin	135	9.9	10
5	000101	-7	5	-7 cos	5 sin	-7 cos+5sin	145	8.6	9
6	000110	-7	1	-7 cos	1 sin	-7 cos+sin	172	7.1	8
7	000111	-7	3	-7 cos	3 sin	-7 cos+3sin	157	7.6	8
8	001000	-5	-7	-5 cos	-7 sin	-5 cos-7sin	235	8.6	9
9	001001	-5	-5	-5 cos	-5 sin	-5 cos-5sin	225	7.1	8
10	001010	-5	-3	-5 cos	-3 sin	-5 cos-3sin	211	5.8	6
11	001011	-5	-1	-5 cos	-1 sin	-5 cos-sin	192	5.1	6
12	001100	-5	7	-5 cos	7 sin	-5 cos+7sin	126	8.6	9
13	001101	-5	5	-5 cos	5 sin	-5 cos+5sin	135	7.1	8
14	001110	-5	1	-5 cos	1 sin	-5 cos +sin	169	5.1	6
15	001111	-5	3	-5 cos	3 sin	-5 cos+3sin	149	5.8	9
16	010000	-1	-7	-1 cos	-7 sin	- cos-7sin	262	7.1	8
17	010001	-1	-5	-1 cos	-5 sin	- cos-5sin	259	5.1	6
18	010010	-1	-3	-1 cos	-3 sin	- cos-3sin	252	3.2	4
19	010011	-1	-1	-1 cos	-1 sin	- cos-sin	225	1.41	2
20	010100	-1	7	-1 cos	7 sin	- cos+7sin	98	7.1	8
21	010101	-1	5	-1 cos	5 sin	- cos+5sin	102	5.1	6
22	010110	-1	1	-1 cos	1 sin	- cos+sin	135	1.41	2
23	010111	-1	3	-1 cos	3 sin	- cos+3sin	109	3.2	4
24	011000	-3	-7	-3 cos	-7 sin	-3 cos-7sin	247	7.6	8
25	011001	-3	-5	-3 cos	-5 sin	-3 cos-5sin	239	5.8	6
26	011010	-3	-3	-3 cos	-3 sin	-3 cos-3sin	225	4.2	5
27	011011	-3	-1	-3 cos	-1 sin	-3 cos-sin	199	3.2	4
28	011100	-3	7	-3 cos	7 sin	-3 cos+7sin	113	7.6	8
29	011101	-3	5	-3 cos	5 sin	-3 cos+5sin	121	5.8	6
30	011110	-3	1	-3 cos	1 sin	-3 cos+sin	174	3.2	4
31	011111	-3	3	-3 cos	3 sin	-3 cos+3sin	135	4.2	5
32	100000	7	-7	7 cos	-7 sin	7 cos-7sin	315	9.9	10
33	100001	7	-5	7 cos	-5 sin	7 cos-5sin	325	8.6	9
34	100010	7	-3	7 cos	-3 sin	7 cos-3sin	337	7.6	8
35	100011	7	-1	7 cos	-1 sin	7 cos-sin	352	7.1	8
36	100100	7	7	7 cos	7 sin	7 cos+7sin	45	9.9	10
37	100101	7	5	7 cos	5 sin	7 cos+5sin	36	8.6	9
38	100110	7	1	7 cos	1 sin	7 cos+sin	9	7.1	8
39	100111	7	3	7 cos	3 sin	7 cos+3sin	24	7.6	8
40	101000	5	-7	5 cos	-7 sin	5 cos-7sin	306	8.6	9
41	101001	5	-5	5 cos	-5 sin	5 cos-5sin	315	7.1	8
42	101010	5	-3	5 cos	-3 sin	5 cos-3sin	329	5.8	6
43	101011	5	-1	5 cos	-1 sin	5 cos-sin	349	5.1	6
44	101100	5	7	5 cos	7 sin	5 cos+7sin	55	8.6	7
45	101101	5	5	5 cos	5 sin	5 cos+5sin	45	7.1	8
46	101110	5	1	5 cos	1 sin	5 cos+sin	12	5.1	6
47	101111	5	3	5 cos	3 sin	5 cos+3sin	31	5.8	6
48	110000	1	-7	1 cos	-7 sin	cos-7sin	278	7.1	8
49	110001	1	-5	1 cos	-5 sin	cos-5sin	282	5.1	6
50	110010	1	-3	1 cos	-3 sin	cos-3sin	289	3.2	4
51	110011	1	-1	1 cos	-1 sin	cos-sin	315	1.41	2
52	110100	1	7	1 cos	7 sin	cos+7sin	82	7.1	8
53	110101	1	5	1 cos	5 sin	cos+5sin	79	5.1	6

54	110110	1	1	1 cos	1 sin	cos+sin	45	1.41	2
55	110111	1	3	1 cos	3 sin	cos+3sin	72	3.2	4
56	111000	3	7	3 cos	7 sin	3 cos+7sin	67	7.6	8
57	111001	3	5	3 cos	5 sin	3 cos+5sin	59	5.8	6
58	111010	3	3	3 cos	3 sin	3 cos+3sin	45	4.2	5
59	111011	3	1	3 cos	1 sin	3 cos+sin	19	3.2	4
60	111100	3	-7	3 cos	-7 sin	3 cos-7sin	293	7.6	8
61	111101	3	-5	3 cos	-5 sin	3 cos-5sin	301	5.8	6
62	111110	3	-3	3 cos	-3 sin	3 cos-3sin	315	4.2	5
63	111111	3	-1	3 cos	-1 sin	3 cos-sin	342	3.2	4

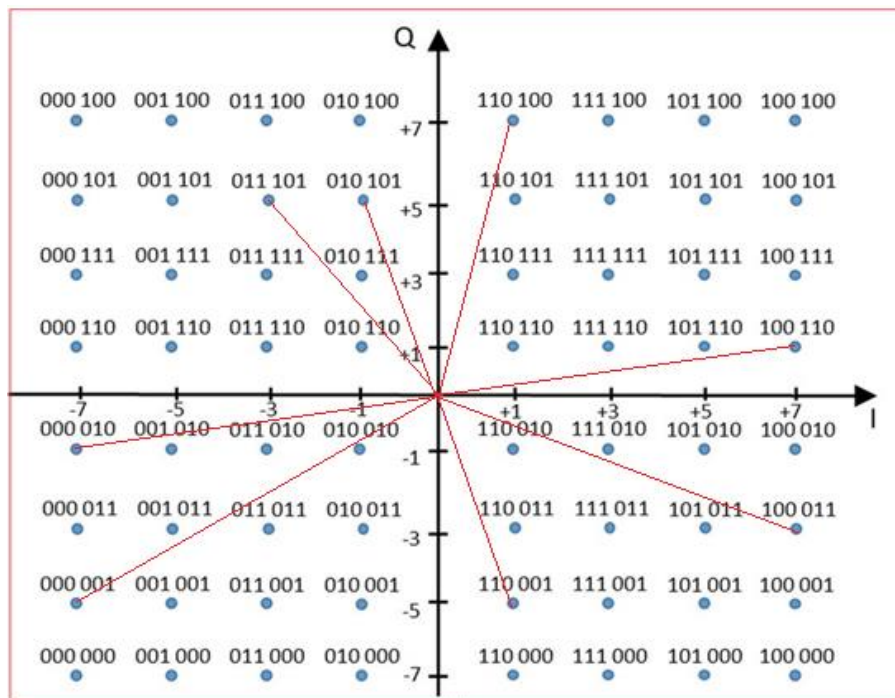


Figure (3) the constellation diagrams of QAM-64 signal

The signal frequency (f) and frequency code (L) of QDDFS is calculated according to the following equations [3]:

$$f = \frac{L \cdot F_{CLK}}{2^n} \quad (6)$$

$$L = \frac{f \cdot 2^n}{F_{CLK}}$$

The functional diagram of digital QAM-64 modulator using QDDFS is shown in figure (4), where every (6) bits are represented by a single signal with its own amplitude and phase, and thus the (6) bits have (64) different combinations, where the three LSB bits represent the (Q) component and the three MSB bits represent the (I) component.

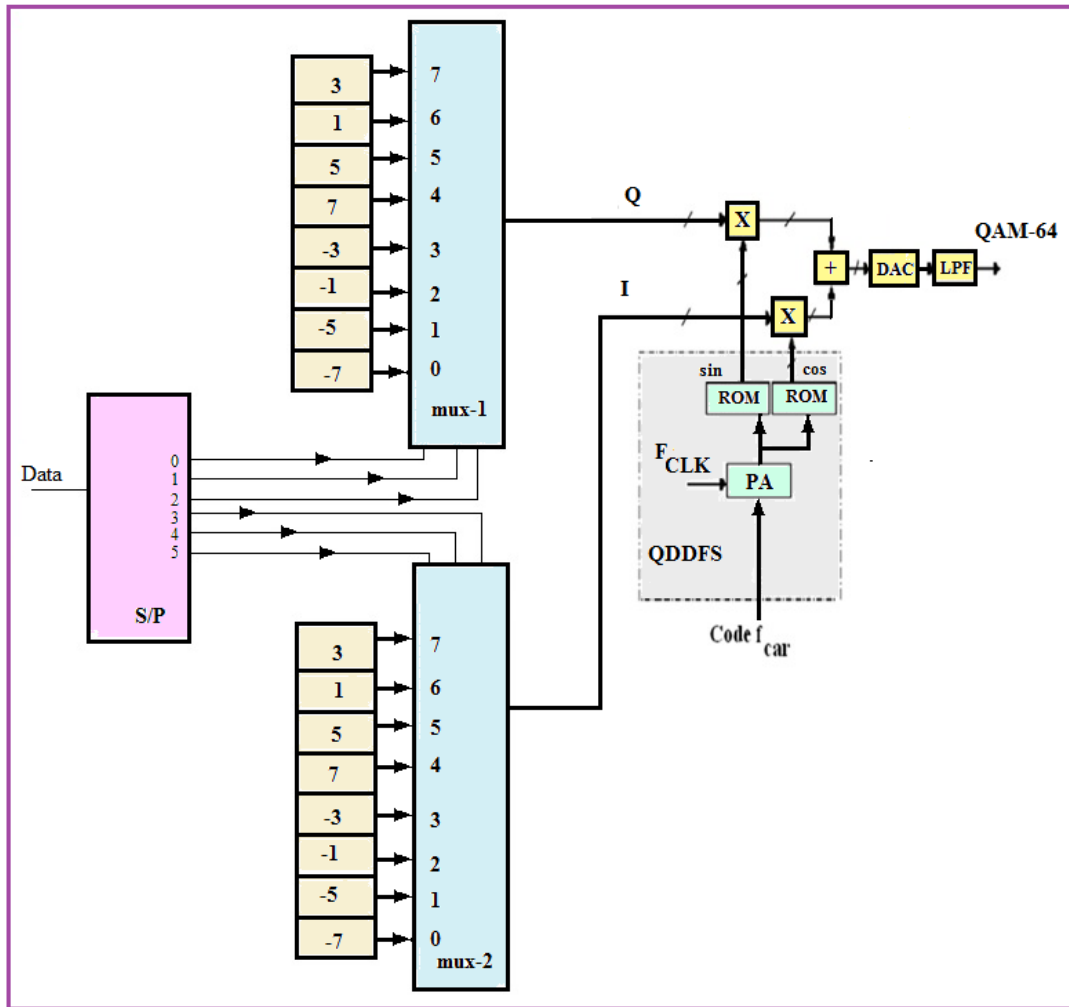


Figure (4) Block diagram of digital QAM-64 using QDDFS

The functional diagram of digital QAM-64 modulator in Quartus II 9.1 design environment is shown in figure (5) where output signals are data signal and QAM-64 signal with the following parameters [9]:

- Clock frequency: $F_{CLK}=50$ MHz
- Modulation type of signal is : QAM-64.
- Carrier frequency of QAM-64 : $f_c= 1$ MHz.
- Frequency of data signal : 1 KHz
- Frequency range of QDDFS : (0.011 Hz...25 MHz).
- Frequency Resolution of QDDFS : (0.011 Hz).
- Size of QDDFS ROM: 2 x 13KB.
- DAC :with 8 bits.
- Bits numbers of Phase Accumulator : $n=32$ bits
- Signal amplitude (5V).

$$\text{For } f = 1 \text{ MHz} \Rightarrow \text{CODE } f = L = \frac{f \cdot 2^n}{F_{CLK}} = \frac{1 \cdot 2^{32}}{50} = 85899346$$

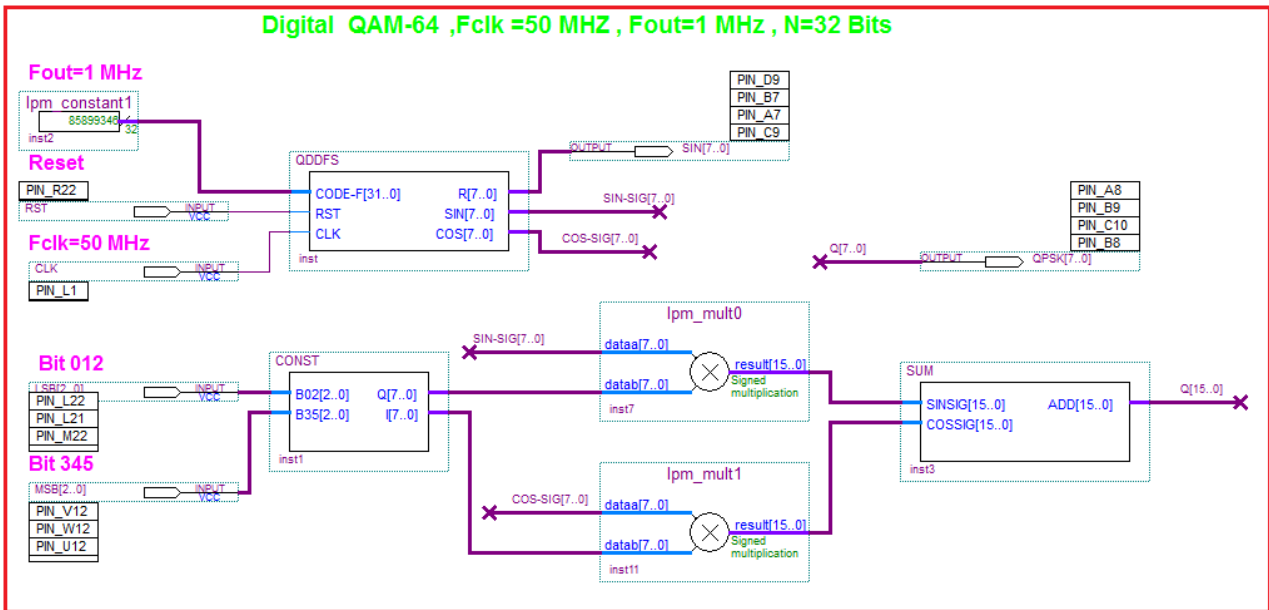


Figure (5) functional diagram of digital QAM-64 in Quartus II 9.1 design environment

V. BLOCK AND FUNCTIONAL DIAGRAMS OF A QDDFS

The QDDFS is assigned to form two signals, the first a sine and the second a cosine, with a phase shift of 90 degrees between them at a frequency of 1 MHz.

The block diagram of digital QDDFS is shown in figure (6), it consists of ROM_SIN for a sine wave and ROM_COS for a cosine waves and phase accumulator with 32 bits, LPF1 (low pass filter), LPF2, DAC1, DAC2 and clock generator ($F_{CLK}=50$ MHz), where L represents the generated frequency code according to the mathematical relation (5).

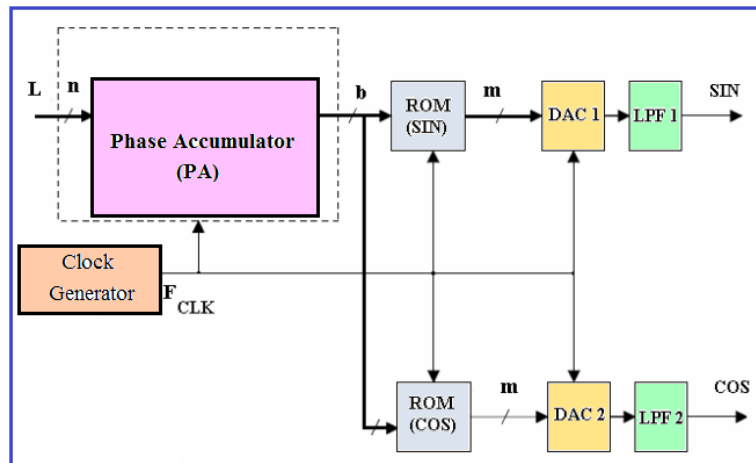


Figure (6) block diagram of QDDFS

The functional diagram of digital QDDFS in Quartus II 9.1 design environment is shown in figure (7), it consists of a sine wave generator and a cosine wave generator.

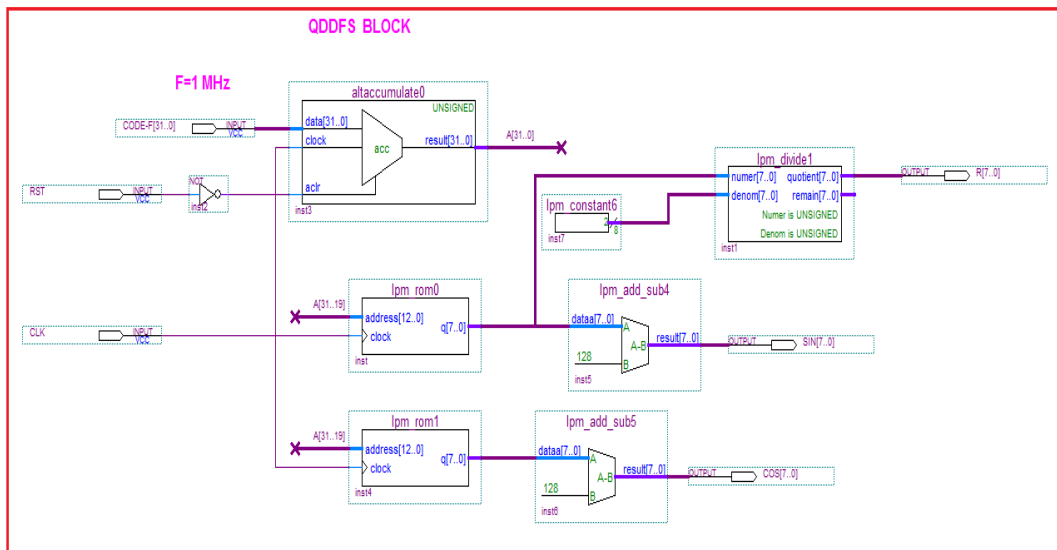


Figure (7) functional diagram of QDDFS in Quartus II 9.1 design environment

The result of designed QDDFS in Quartus II 9.1 design environment is shown in figure (8) in time domains, where carrier frequency of signals 1MHz and phase shift is 90° .

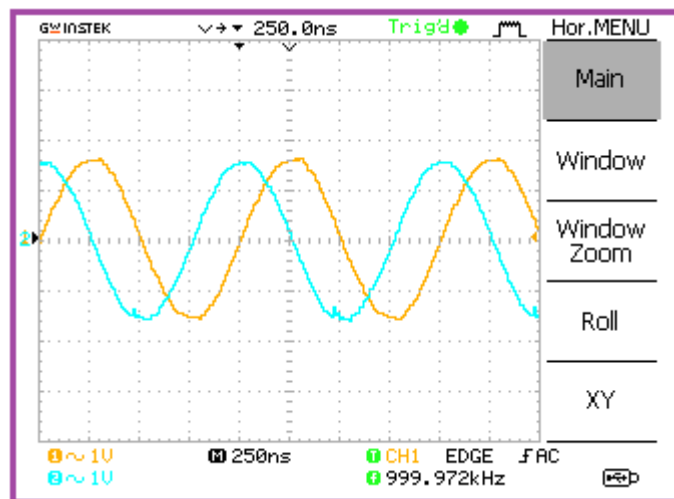


Figure (8) quadrature signals (sin and cos) in time and

VI. FUNCTIONAL DIAGRAMS OF A CONSTANT BLOCK (CONST)

The block of constants is assigned to form the constants (7, -7, 5, -5, 3, -3, 1, -1) for the (Q) and (I) components. The functional diagram of Constant block (CONST) in Quartus II 9.1 design environment is shown in figure (9).

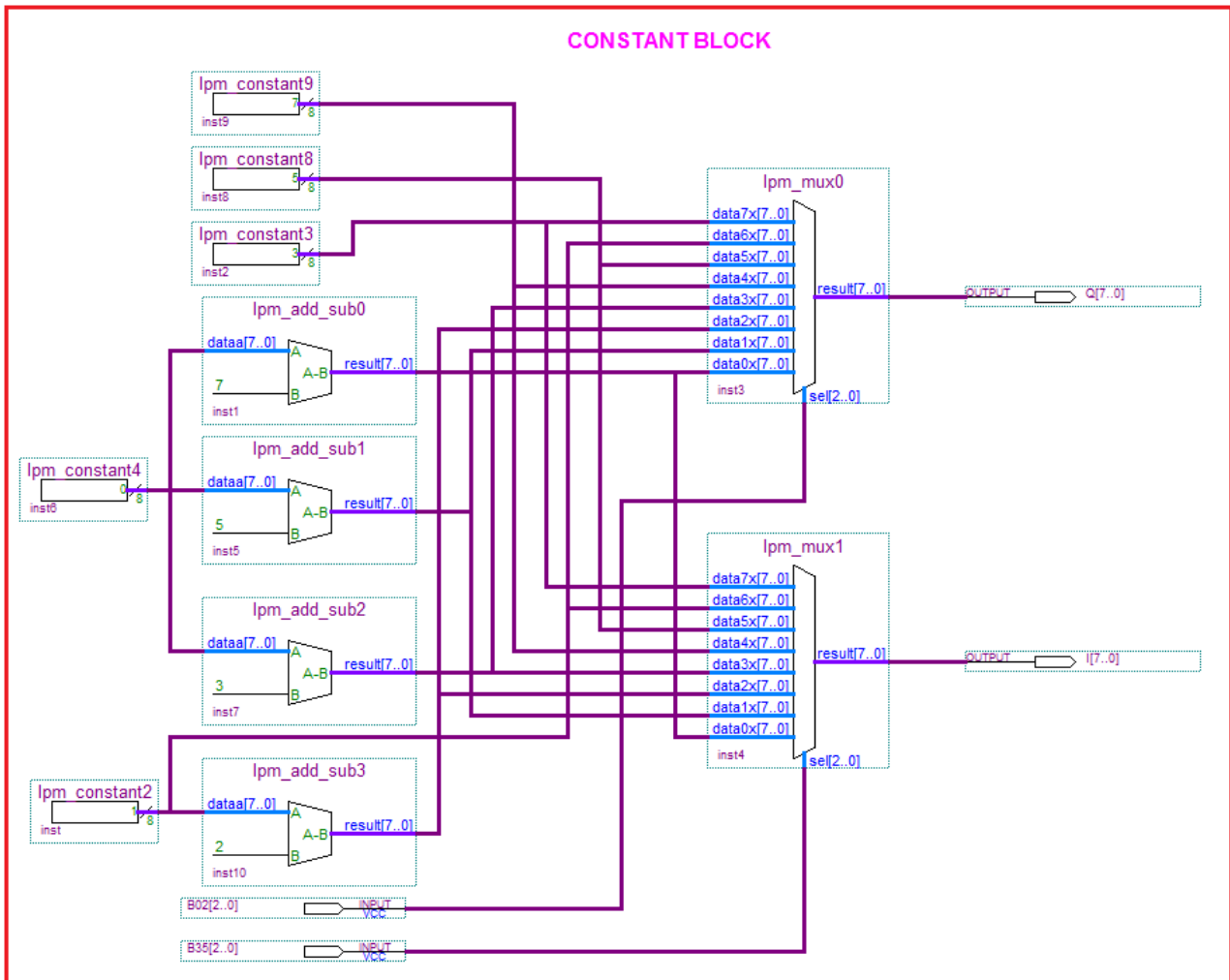


Figure (9) functional diagram of constant block in Quartus II 9.1 design environment

VII. FUNCTIONAL DIAGRAMS OF A SUMMATION BLOCK (SUMM)

The sum block is dedicated to forming the following sum signal:

$$U_{QAM-64}(t) = I.\cos(2\pi f t) + Q.\sin(2\pi f t)$$

$$I = \mp 1 \text{ or } \pm 3 \text{ or } \pm 5 \text{ or } \pm 7 \text{ and } Q = \mp 1 \text{ or } \pm 3 \text{ or } \pm 5 \text{ or } \pm 7$$

and also to adjust the scales of the sum signal values so that their digital values are within the limits of the DAC used in the design.

The functional diagram of sum block (CONST) in Quartus II 9.1 design environment is shown in figure (10).

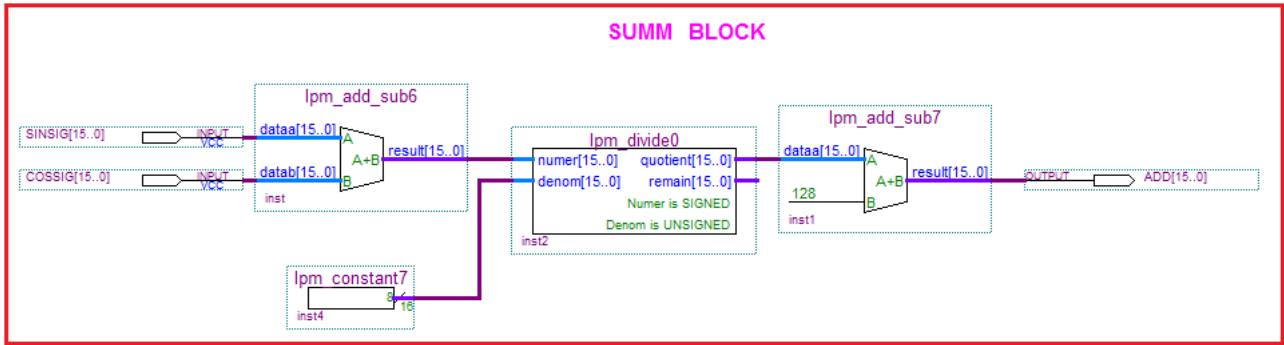


Figure (10) functional diagram of summation block in Quartus II 9.1 design environment

The result of designed digital QAM-64 modulator in Quartus II 9.1 design environment is shown in figure (11-a , b , c , d) in time domains , where frequency of data signal : 1 KHz , carrier frequency of QAM-64 : 1 MHz , phase shift and amplitude of QAM-64 signals is shown in table .2.

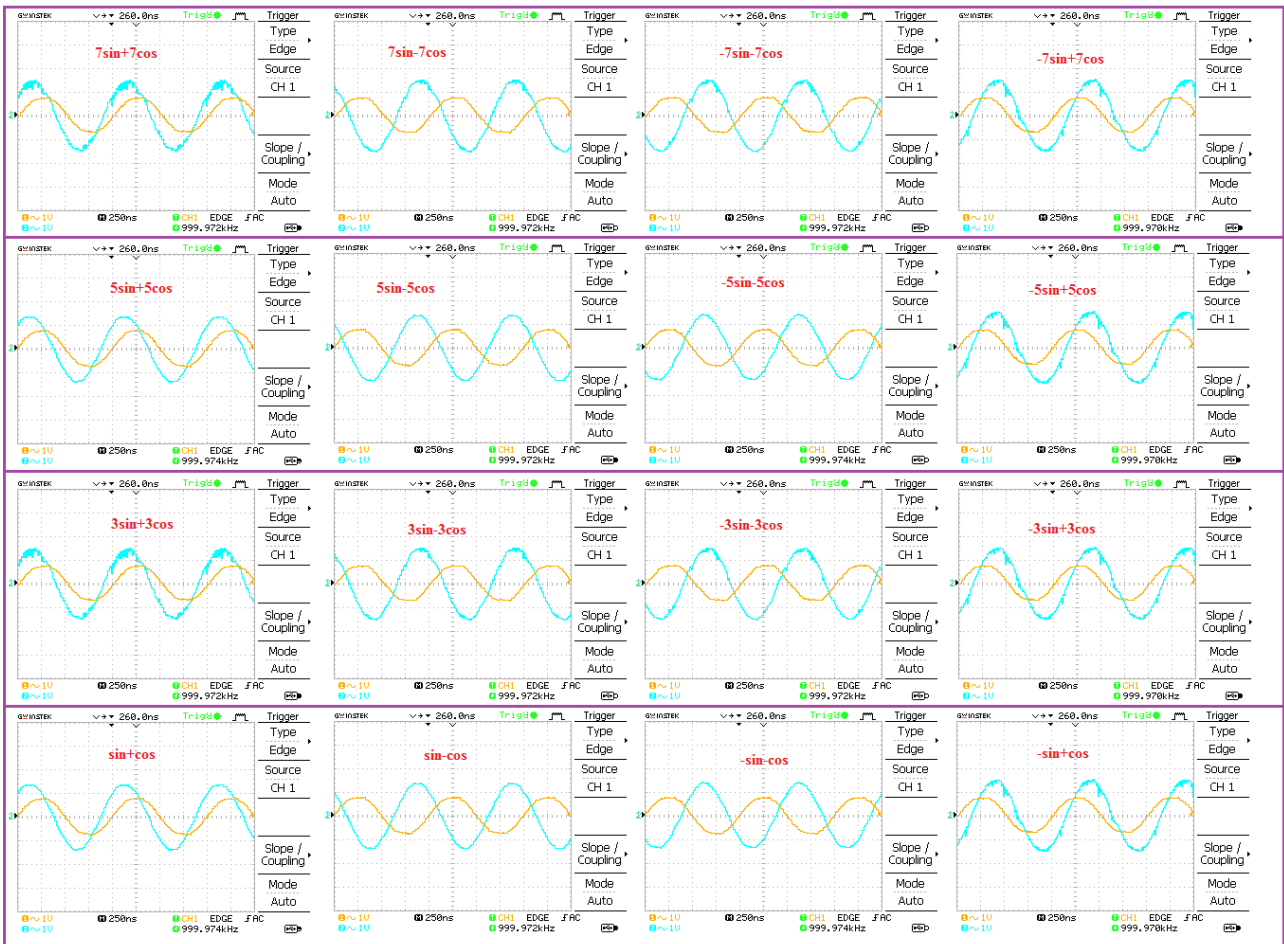


Figure (11-a) QAM-64 signals in time domain according values of table.2

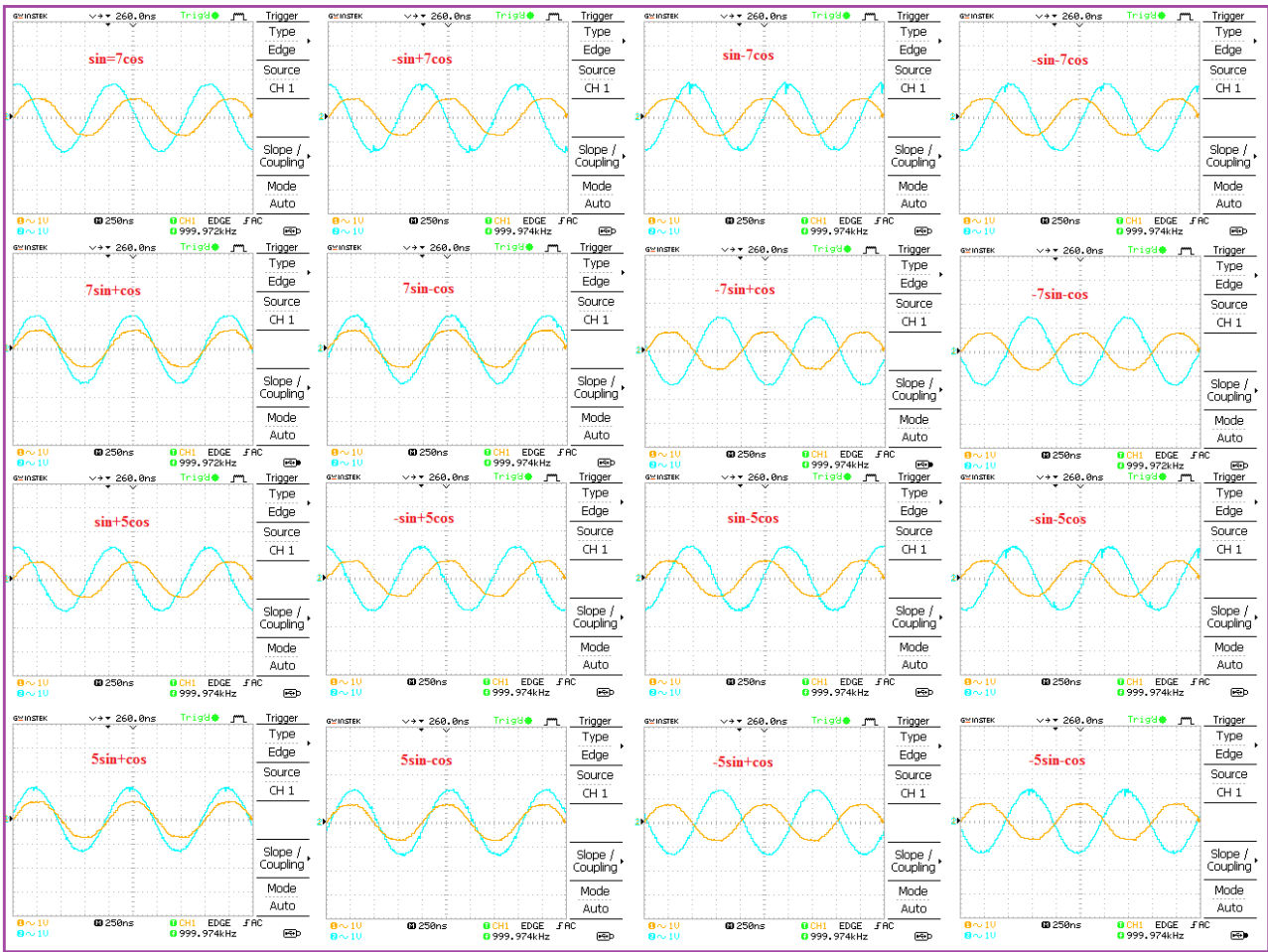


Figure (11-b) QAM-64 signals in time domain according values of table.2

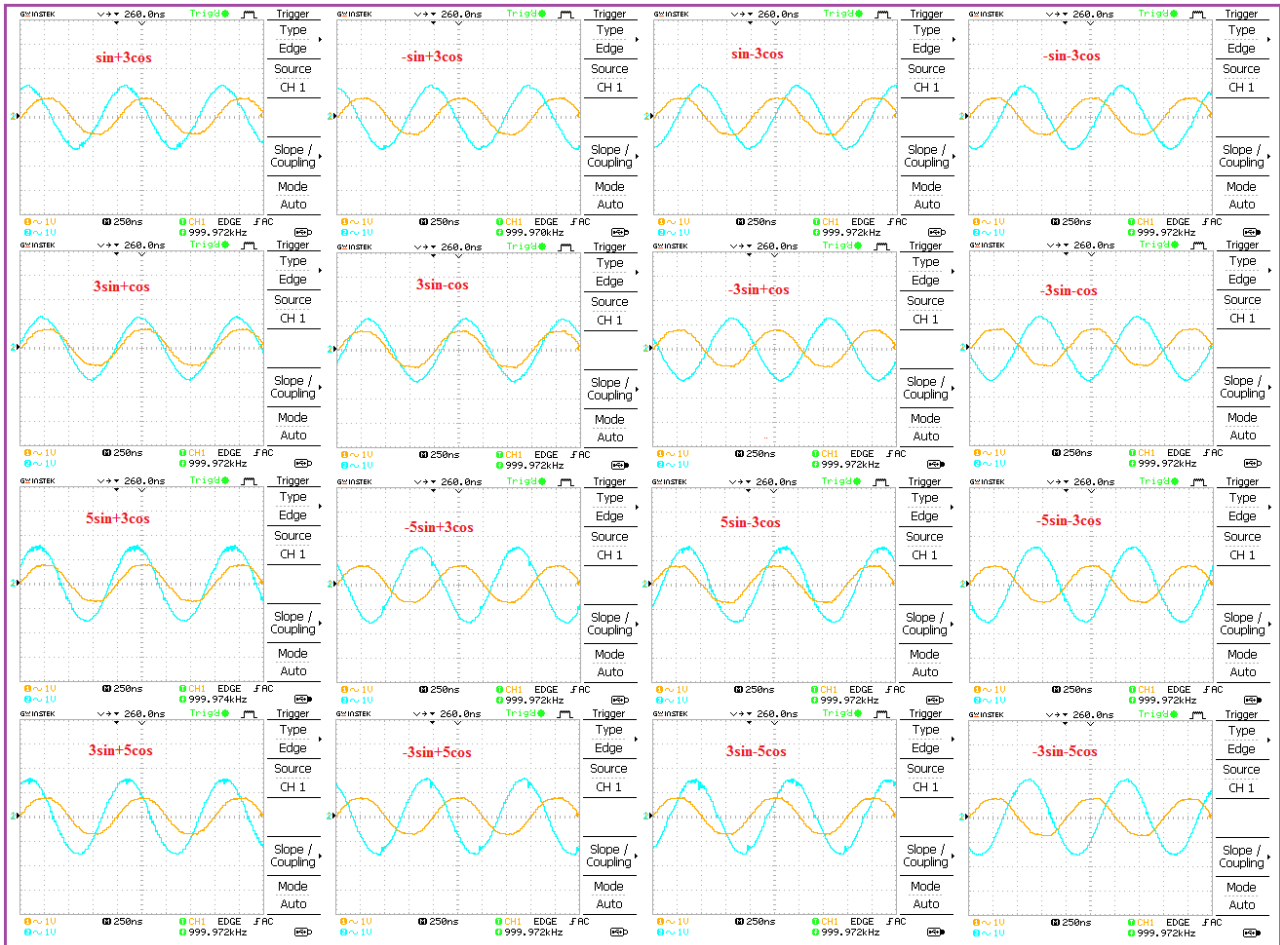


Figure (11-c) QAM-64 signals in time domain according values of table.2



Figure (11-d) QAM-64 signals in time domain according values of table.2

VIII. DISCUSSION AND CONCLUSION

- Depending on the previous practical results, the digital QAM-64 were successfully designed using FPGA.
- In this research, the digital modulators were designed with QDDFS which is considered as a highly accuracy technique in carrier sinusoidal, data signal, and QAM-64 synthesizing on FPGA chips.
- Practical experiments described in the study suggest how these modulators can be used in real communication devices.
- There is a possibility to develop this algorithm through designing digital QAM-128, QAM-256 and another modulators types.

REFERENCES

- [1] Fuqin Xiong digital Modulation Techniques, -(Artech House telecommunications library) ,/653/ pages., 2000
- [2] www.complextoreal.com (All About Modulation –Part I)
- [3] Goldberg, "Digital Frequency Synthesis Demystified";1999.
- [4] Advances in Computer Science Research ,volume 78, 3rd International Workshop on Materials Engineering and Computer Science Research (IWMECS 2018).
- [5]MOLABANTI PRAVEEN KUMAR, T.S.R KRISHNA PRASAD, M .VIJAYA KUMA , Implementation of Digital Communication Laboratory on FPGA, International Journal of Advanced Research in Computer and Communication Engineering ,Vol. 2, Issue 11, November 2013
- [6] ALTERA, CORPORATION, " Cyclone II Device Family Data Sheet"; 2005.
- [7] ALTERA, CORPORATION, " Cyclone II FPGA Starter Development Board";2003.
- [8] Dr. Kamal Aboutabikh, Dr. Ibrahim Haidar, Dr. Amer Garib, Design and Implementation of a Digital FIR LPF with Variable Pass-Band for ECG Signal using FPGA, International Journal of Advanced Research in Computer and Communication Engineering Vol. 4, Issue 9, September 2015.

[9] Volnei A. Pedroni, Circuit Design With VHDL, MIT Press Cambridge, Massachusetts London, England (2004) 364.

BIOGRAPHY



Dr. Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR , university of communication in Leningrad , holds a degree assistant professor in 2009 from Aleppo university.

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