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Design and Implementation of a Digital Quadrature Amplitude Modulator QAM-16 using FPGA

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Abstract: In this paper, we propose the design and implementation mechanism for different digital modulators such as Quadrature Amplitude QAM-16 modulators based on the use of Quadrature Direct Digital Frequency Synthesizer (QDDFS) using Cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1 with the following parameters:

- Clock frequency : FCLK=50MHz .
- Modulation type of signal is : QAM-16 .
- Frequency range : (0.011 Hz…10 MHz) .
- Frequency Resolution : (0.011 Hz) .
- Signal amplitude (5V) .
- Data frequency : 1KHz .
- Digital designs allow the slides to modify and design development for results and better through reprogramming, depending on the user's desire.

Keywords: Digital Modulator**,** QAM, QAM-16, DDFS, QDDFS, FPGA.

I. INTRODUCTION

The mathematical principle of digital QAM modulation using QDDFS can be explained according to the diagram [1] shown in figure (1), where the Quadrature Amplitude Modulation achieved on multiply of data signal and samples of sinusoidal and cosine signals [2] stored in ROMs of QDDFS .

QAM-16 modulation achieved on adding (I. cos w_c t) and (Q. sin w_c t) signals from the QDDFS , where: I=1 or -1 or 3 or -3 and Q=1 or -1 or 3 or -3.

The stored values of the sine and cosine signals in ROM of DDFS and QDDFS are calculated according to the following equation [3]:

$$U_{\sin}(i) = INT\left[\left(2^{m-1}-1\right).\sin\left(\frac{360.i}{2^b}\right)\right] \qquad (1)$$

$$U_{\cos}(i) = INT\left[\left(2^{m-1}-1\right).\cos\left(\frac{360.i}{2^b}\right)\right]$$

For:

$$\mathrm{m} = 8\,\mathrm{bits}\,,\ \mathrm{b} = 13\,\mathrm{bits}\,,\ i = (0....2^b-1) = (0...8191)$$

Then:

$$U_{\sin}(i) = INT\left[\left(2^{8-1}-1\right).\sin\left(\frac{360.i}{2^{13}}\right)\right] = INT\left[127.\sin\left(\frac{360.i}{8192}\right)\right]$$

$$U_{\cos}(i) = INT\left[\left(2^{8-1}-1\right).\cos\left(\frac{360.i}{2^{13}}\right)\right] = INT\left[127.\cos\left(\frac{360.i}{8192}\right)\right]$$

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$$U_{\sin}(i) = (-127 \ldots\ldots +127)$$
$$U_{\cos}(i) = (-127 \ldots\ldots +127)$$

To avoid negative values that are difficult to store in memory, we add a value off-set= 128

$$U_{\sin}(i) = (0 \ldots\ldots 255)$$
$$U_{\cos}(i) = (0 \ldots\ldots 255)$$

In paper [4] present the design and simulation only of a modulation module for ASK using VHDL.
In paper [5] present the design and simulation of a modulation module for ASK ,FSK,BPSK,QPSK using VHDL.

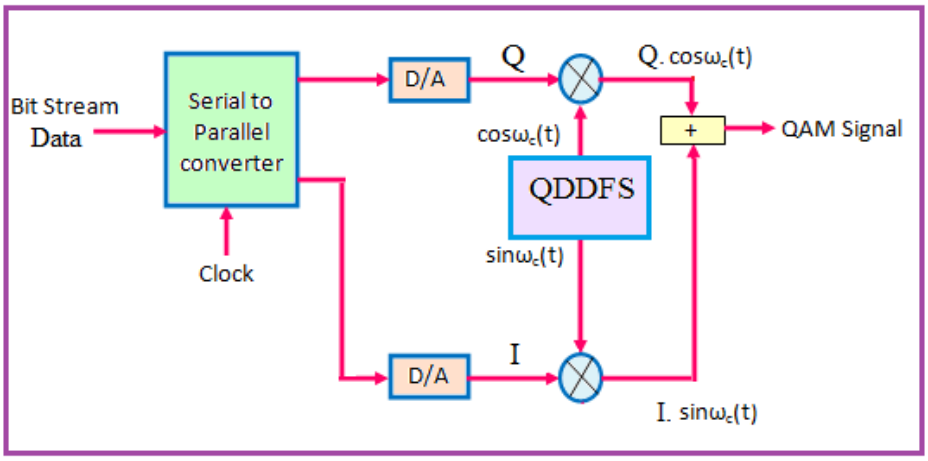

Fig (1) Block diagram of digital QAM modulator using QDDFS

II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

-In this paper digital QAM-16 modulator were designed, implemented and tested based on the use of Quadrature Digital Direct Frequency Synthesizer (QDDFS) using FPGA, VHDL and Graphical programming language with Quartus II 9.1 design environment.

-Using the digital QDDFS with mathematical operations (adding , multiply , division) , makes the digital modulation design process flexible, accurate and highly efficient.

-Changing the data signal frequency , carrier signal frequency, frequency deviation and phase shift within different values explains the difference between digital modulation and analog modulation .

III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the digital modulators for different modulation types of signals, the following tools and software are used:

-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [6].
-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.
-VHDL programming language with Quartus II 9.1 design environment [7].
-Design Environment MATLAB R2008a
-GDS-1052 digital oscilloscope with Free Wave program to take the results .
-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [8] is shown in figure (2).

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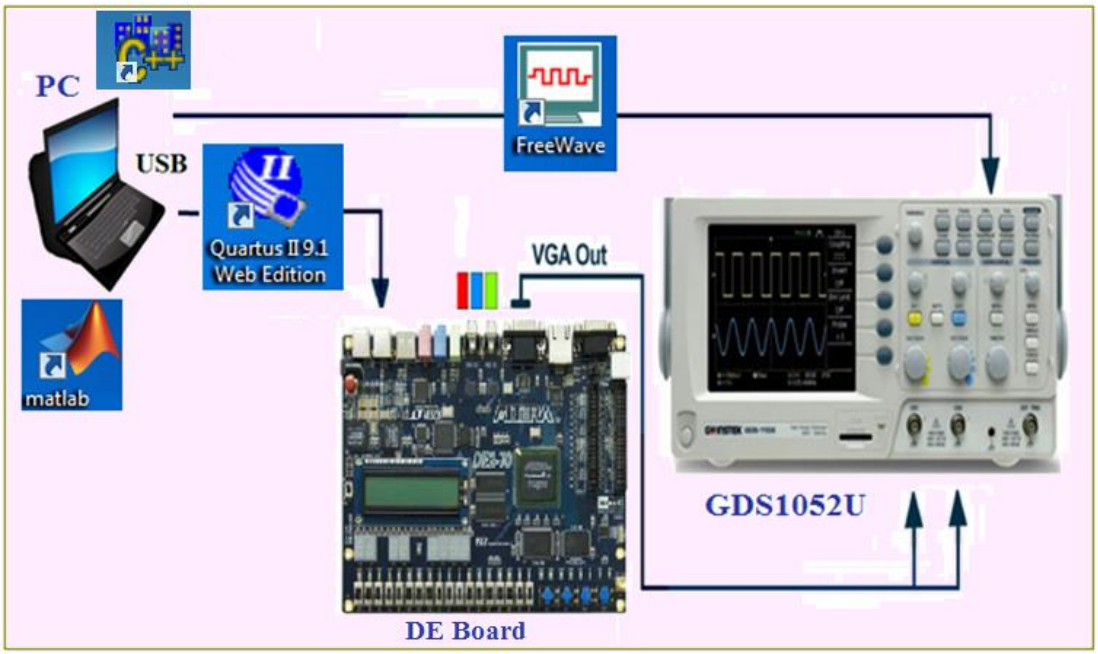

Fig (2) Block diagram of the laboratory experiment platform

IV. BLOCK AND FUNCTIONAL DIAGRAMS OF A DIGITAL QAM-16 MODULATOR

The characteristics of QAM types is shown in table 1:

Table.1 : types of QAM

Name of scheme	Bit per symbol (bits)	Number of symbols
QAM-4	2	2^2=4
QAM-8	3	2^3=8
QAM-16	**4**	**2^4=16**
QAM-32	4	2^5=32
QAM-64	6	2^6=64

The QAM-16 signal is given according to the fallowing equation [3] :

$$U_{QAM-16}(t) = \mathrm{I}.\cos(2\pi\ f_c\ t) + \mathrm{Q}.\sin(2\pi\ f_c\ t)\ \ ,\mathrm{I} = \mp 1\ \text{or}\ \pm 3\ \text{and}\ \mathrm{Q} = \pm 1\ \text{or}\ \pm 3 \qquad (2)$$
$$U_{QAM-16}(t) = A.\sin(2\pi\ f_c\ t + \theta)$$

Where:

$$\text{Amplitude} = \mathrm{A} = \sqrt{(I)^2 + (Q)^2} = \sqrt{I^2 + Q^2} \qquad (3)$$

$$\text{Phase} = \theta = tan^{-1}\left(\frac{Q}{I}\right) \qquad (4)$$

Where: $I = \pm 1\ , \pm 3\ \ ,\ Q = \pm 1\ , \pm 3$, (w_c) carrier frequency of signal.

Values of Data (0000, …… ,1111) , I component , Q component , QAM-16 output signal ,amplitude and phase QAM-16 given according to the table .2 , the constellation diagrams of QAM-16 signal shown in figure (3).

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Table .2 : values of : I, Q, QAM-16, Phase and Amplitude QAM-16									
N	**Data**	**Q**	**I**	**Q*sin**	**I*cos**	**Out**	**Phase**	**Amplitude**	**Scale factor**
0	0000	+3	+3	+3 sin	+3 cos	+3 sin+3 cos	45	$3\sqrt{2} = 4.243$	5
1	0001	+3	+1	+3 sin	+ cos	+3 sin + cos	71.6	$\sqrt{10} = 3.2$	4
2	0010	+3	-3	+3 sin	-3 cos	+3 sin -3 cos	135	$3\sqrt{2} = 4.243$	5
3	0011	+3	-1	+3 sin	- cos	+3 sin - cos	108.4	$\sqrt{10} = 3.2$	4
4	0100	-3	+3	-3 sin	+3 cos	- 3 sin +3 cos	315	$3\sqrt{2} = 4.243$	5
5	0101	-3	+1	-3 sin	+ cos	-3 sin + cos	288.4	$\sqrt{10} = 3.2$	4
6	0110	-3	-3	-3 sin	-3 cos	-3 sin -3 cos	225	$3\sqrt{2} = 4.243$	5
7	0111	-3	-1	-3 sin	- cos	-3 sin - cos	251.6	$\sqrt{10} = 3.2$	4
8	1000	+1	+3	+ sin	+3 cos	+ sin +3 cos	18.4	$\sqrt{10} = 3.2$	4
9	1001	+1	+1	+ sin	+ cos	+ sin + cos	45	$\sqrt{2} = 1.41$	2
10	1010	+1	-3	+ sin	-3 cos	+ sin - 3cos	161..6	$\sqrt{10} = 3.2$	4
11	1011	+1	-1	+ sin	- cos	+ sin - cos	135	$\sqrt{2} = 1.41$	2
12	1100	-1	+3	- sin	+3 cos	+3 sin - cos	341.6	$\sqrt{10} = 3.2$	4
13	1101	-1	+1	- sin	+ cos	+ sin - cos	315	$\sqrt{2} = 1.41$	2
14	1110	-1	-3	- sin	-3 cos	- sin – 3 cos	198.4	$\sqrt{10} = 3.2$	4
15	1111	-1	-1	- sin	- cos	- sin - cos	225	$\sqrt{2} = 1.41$	2

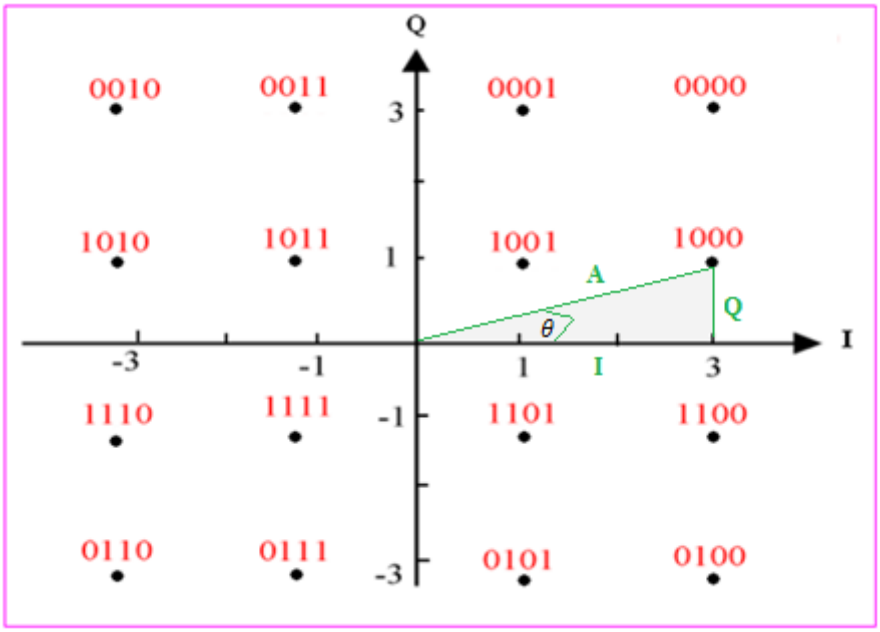

Fig (3) the constellation diagrams of QAM-16 signal

The signal frequency (f) and frequency code (L) of DDFS is calculated according to the fallowing equations [3]:

$$f = \frac{L.F_{CLK}}{2^n} \qquad (5)$$

$$\mathrm{L} = \frac{f.2^n}{F_{CLK}}$$

The functional diagram of digital QAM-16 modulator using QDDFS is shown in figure (4), where every 4 bits are represented by a single signal with its own amplitude and phase, and thus the 4 bits have 16 different combinations, where the two LSB bits represent the (I) component and the two MSB bits represent the (Q) component.

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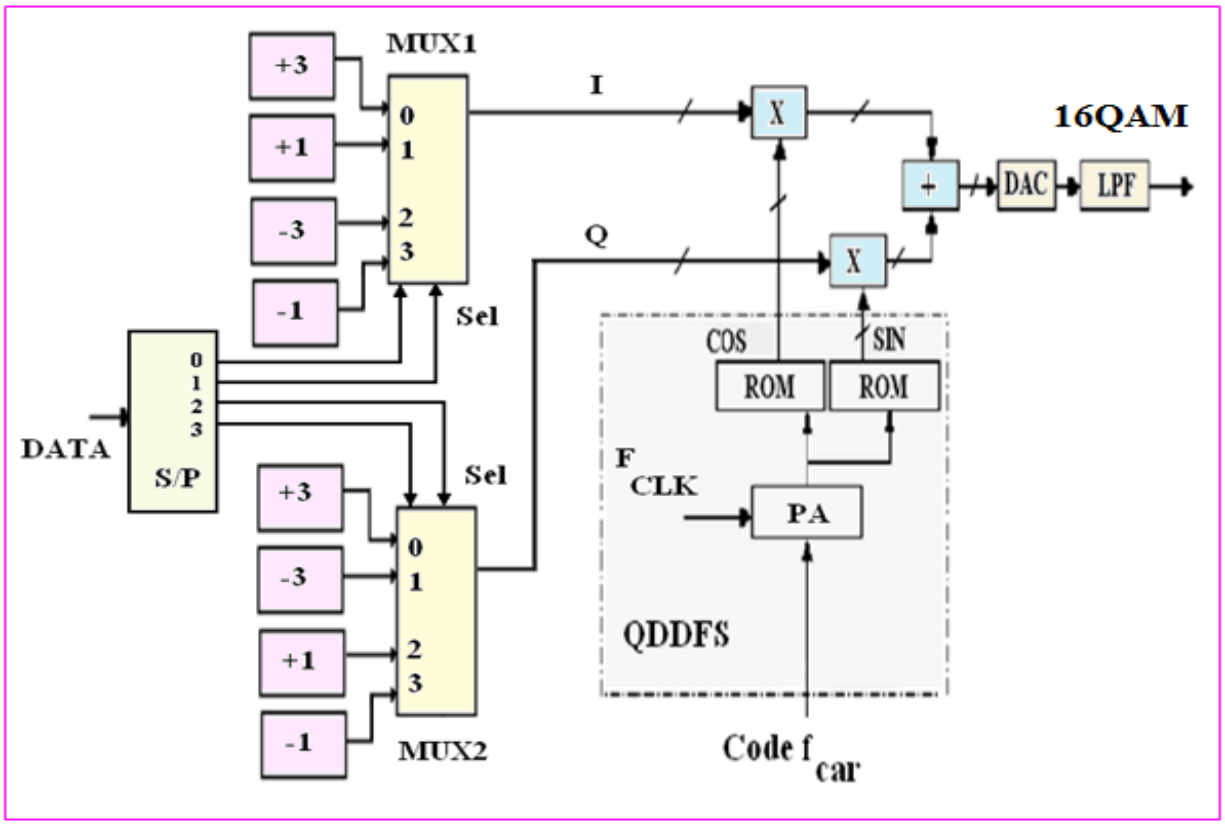

Fig (4) Block diagram of digital QAM-16 using QDDFS

The functional diagram of digital QAM-16 modulator in Quartus II 9.1 design environment is shown in figure (5). It consists of : QDDFS block , constant block and summation block ,where output signals of block diagram of digital QAM-16 are :

data signal and QAM-16 signal with the following parameters **[**9**]:**

-Clock frequency: F_{CLK}=50 MHz
-Modulation type of signal is : QAM-16.
-Carrier frequency of QAM-16 : f= 1 MHz.
-Frequency of data signal : 1 KHz
-Frequency range of QDDFS : (0.011 Hz…25 MHz).
-Frequency Resolution of QDDFS : (0.011 Hz).
-Size of QDDFS ROM: 2 x 13KB.
-DAC :with 8 bits.
-Bits numbers of Phase Accumulator : n=32 bits
-Signal amplitude (5V).

$$For \quad \mathrm{f} = 1\,\mathrm{MHz} \Rightarrow CODE\ \mathrm{f} = L = \frac{f.2^{n}}{F_{CLK}} = \frac{1*2^{32}}{50} = 85899346$$

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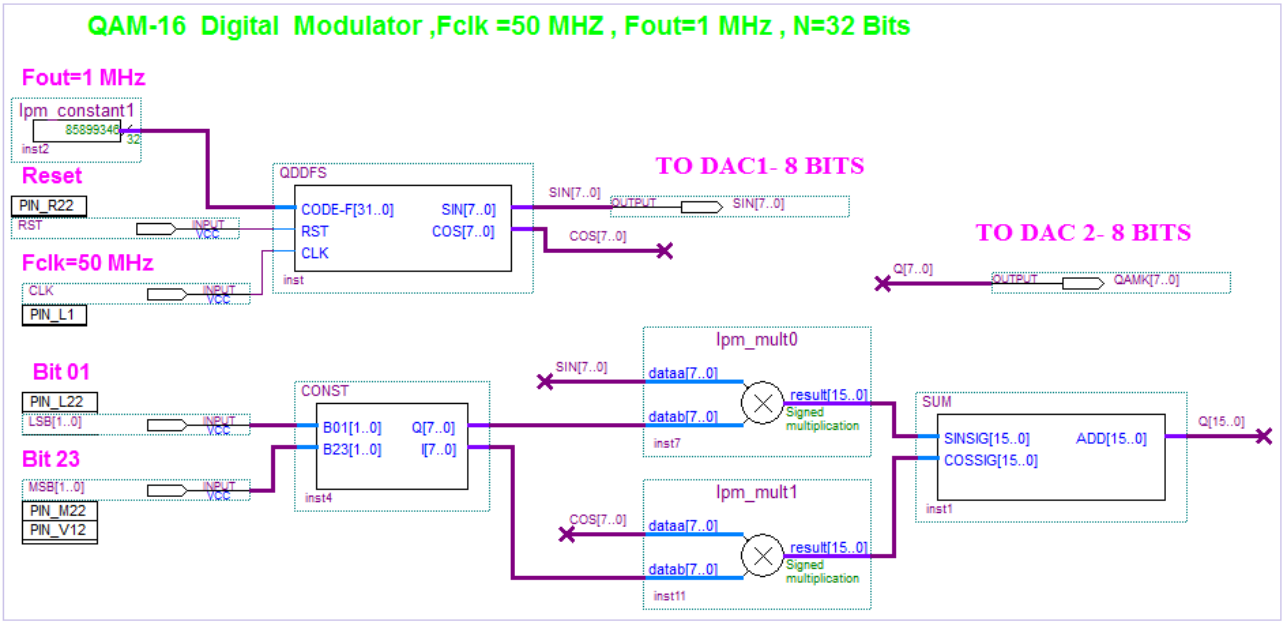

Fig (5) functional diagram of digital QAM-16 modulator in Quartus II 9.1 design environment

V. BLOCK AND FUNCTIONAL DIAGRAMS OF A QDDFS

The QDDFS is assigned to form two signals, the first a sine and the second a cosine, with a phase shift of 90 degrees between them at a frequency of 1 MHz.

The block diagram of digital QDDFS is shown in figure (6) , it is consists of ROM_SIN for a sine wave and ROM_COS for a cosine waves and phase accumulator with 32 bits , LPF1 (low pass filter) , LPF2 , DAC1 ,DAC2 and clock generator (F_{CLK}=50 MHz) , where L represents the generated frequency code according to the mathematical relation (5).

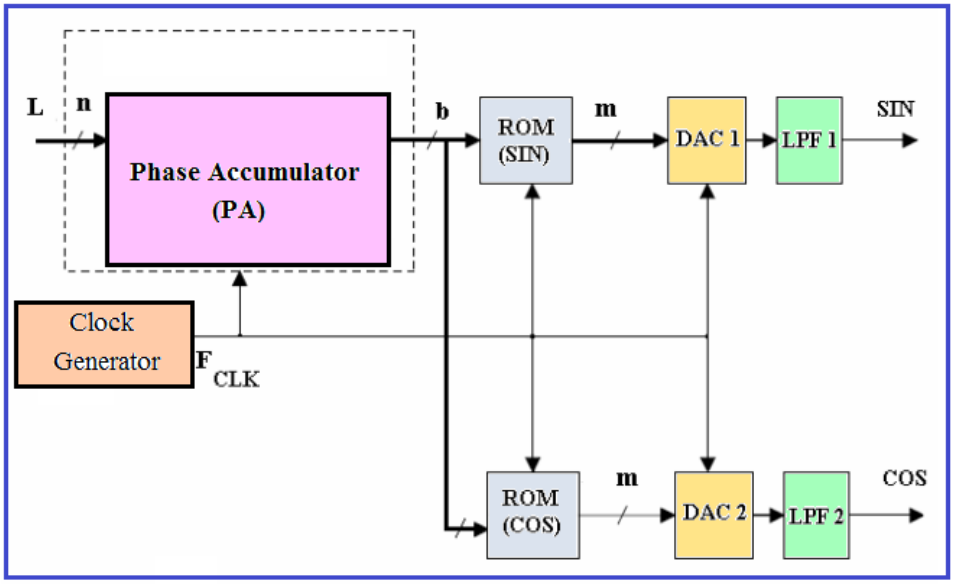

Fig (6) block diagram of QDDFS

The functional diagram of digital QDDFS in Quartus II 9.1 design environment is shown in figure (7) , it is consists of a sine wave generator and a cosine wave generator.

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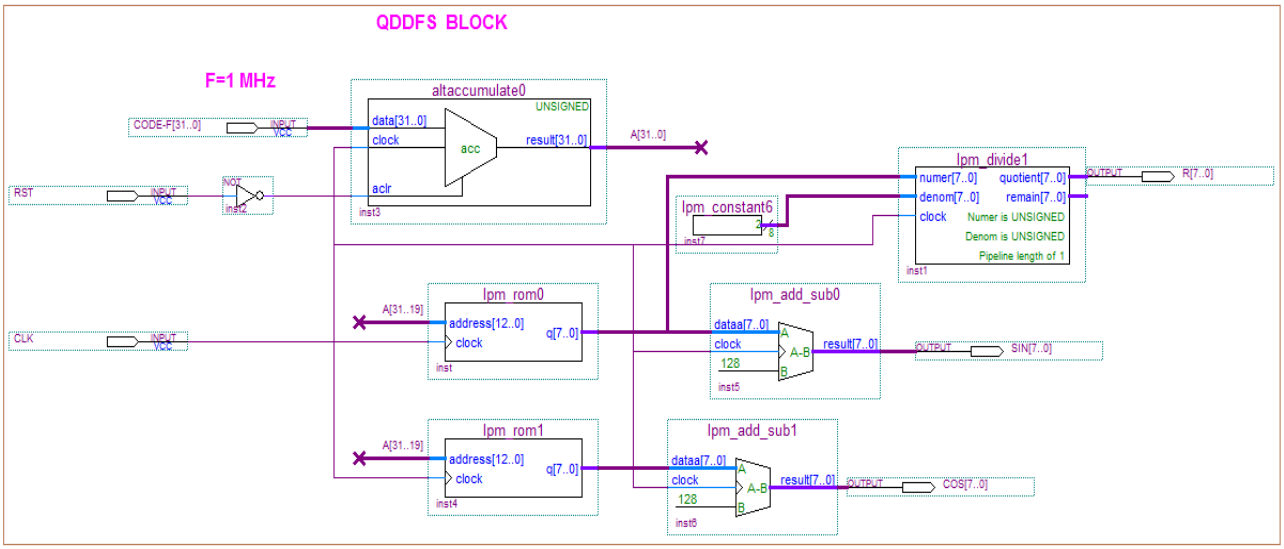

Fig (7) functional diagram of QDDFS in Quartus II 9.1 design environment

The result of designed QDDFS in Quartus II 9.1 design environment is shown in figure (8) in time domain , where carrier frequency of signals 1MHz and phase shift is (90^0).

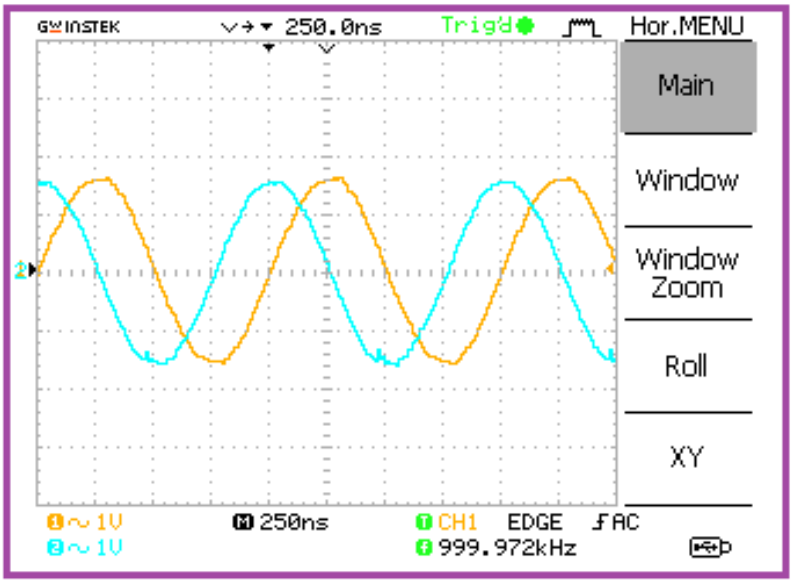

Fig (8) quadrature signals (sin and cos) in time domain

VI. FUNCTIONAL DIAGRAMS OF A CONSTANT BLOCK (CONSTANT)

The block of constants is assigned to form the constants (3,-3,1, -1) for the (Q) and (I) components.

The functional diagram of Constant block (CONSTANT) in Quartus II 9.1 design environment is shown in figure (9) .

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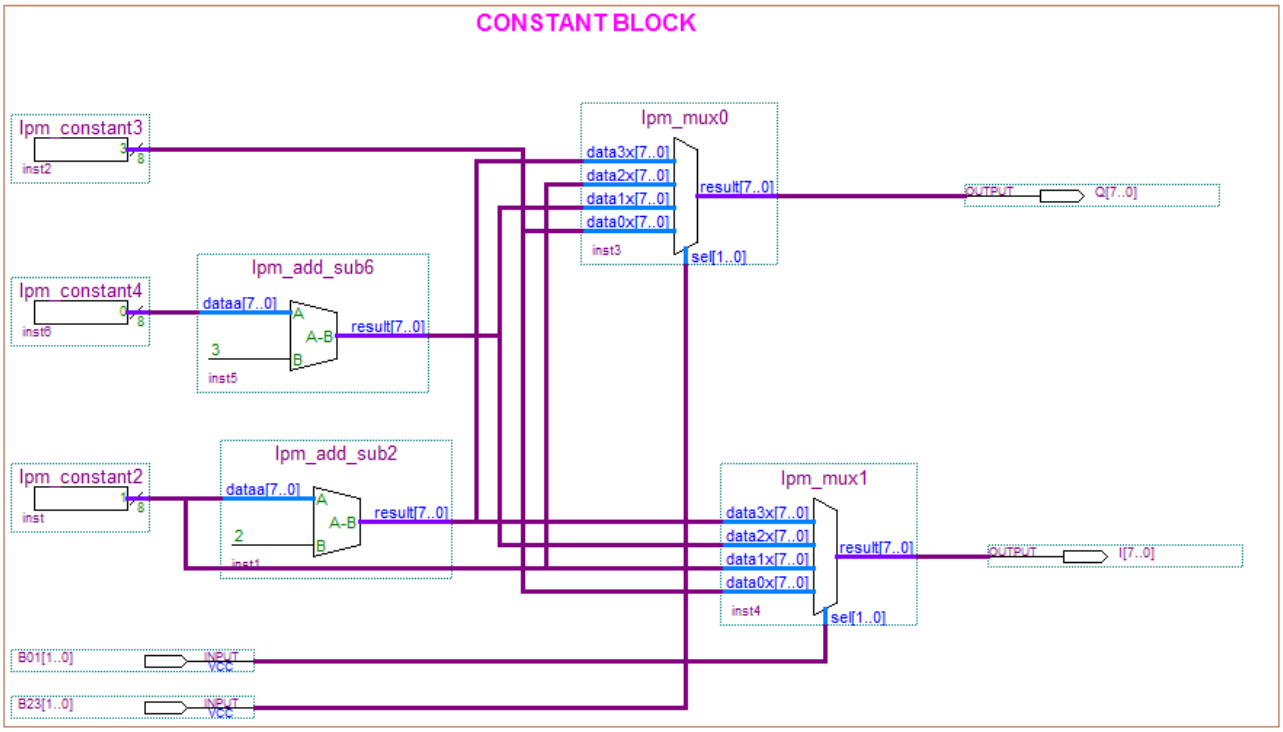

Fig (9) functional diagram of constant block in Quartus II 9.1 design environment

VII. FUNCTIONAL DIAGRAMS OF A SUMMATION BLOCK

The sum block is dedicated to forming the following sum signal:

$$U_{QAM-16}(t) = \mathrm{I}.\cos(2\pi\ f\ t) + \mathrm{Q}.\sin(2\pi\ f\ t)\ \ , \mathrm{I} = \mp 1 \text{ or} \pm 3 \text{ and } \mathrm{Q} = \pm 1 \text{ or } \pm 3$$

and also to adjust the scales of the sum signal values so that their digital values are within the limits of the DAC used in the design.

The functional diagram of sum block (CONST) in Quartus II 9.1 design environment is shown in figure (10) .

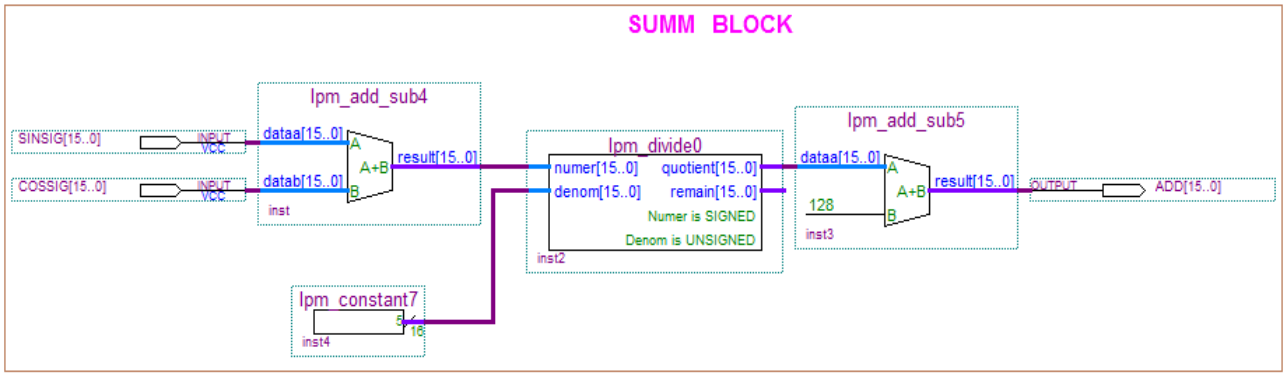

Fig (10) functional diagram of summation block in Quartus II 9.1 design environment

The result of designed digital QAM-16 modulator in Quartus II 9.1 design environment is shown in figure (11) in time domains , where frequency of data signal : 1 KHz , carrier frequency of QAM-16 : 1 MHz , phase shift : 45^0 , 135^0 , 225^0, 315^0,71.6^0,18.4,108.4^0 ,288.4^0 , 251.6^0 , 161.6^0 , 341.6 ^{0}, 198.4^0.

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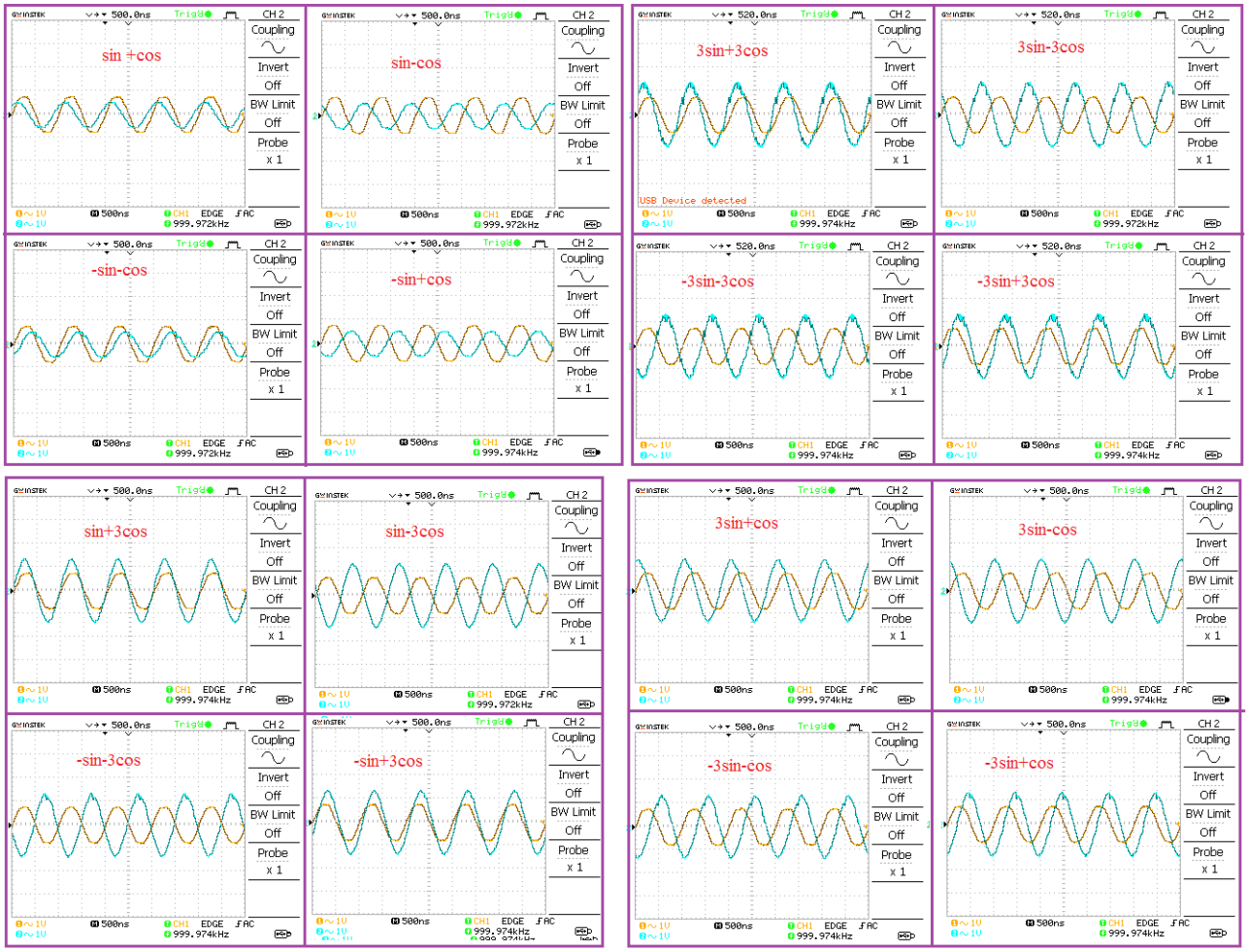

Fig (11) QAM-16 signals in time domains according values of table.2

VIII. DISCUSSION AND CONCLUSION

- Depending on the previous practical results ,the digital QAM-16 modulator were successfully designed using FPGA.

- In this research, the digital modulators were designed with QDDFS which is considered as a highly accuracy technique in carrier sinusoidal , data signal, and QAM-16 synthesizing on FPGA chips.

- Practical experiments described in the study suggest how these modulators can be used in real communication devices.

- There is a possibility to develop this algorithm through designing digital QAM-64 and QAM-128,QAM-256 and another modulators types.

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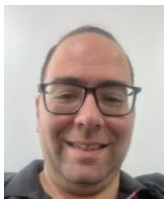

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