International Multidisciplinary Research Journal Reviews (IMRJR)

International Multidisciplinary Research Journal Reviews (IMRJR)
A Peer-reviewed journal
Volume 1, Issue 1, September 2024
DOI 10.17148/IMRJR.2024.010107

Design and Implementation of a Digital Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), Binary Phase Shift Keying(BPSK) and Quadrature Phase Shift Keying (QPSK) Modulators using FPGA

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Abstract: In this paper, we propose the design and implementation mechanism for different digital modulators such as Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK) modulators based on the use of Direct Digital Frequency Synthesizer (DDFS) and QDDFS using Cyclone II EP2C20F484C7 FPGA from ALTERA placed on education and development board DE-1 with the following parameters

- Clock frequency : F_{CLK}=50MHz .
- Modulation type of signal is :ASK ,FSK , BPSK , QPSK .
- Frequency range : (0.011 Hz…10 MHz) .
- Frequency Resolution : (0.011 Hz) .
- Signal amplitude(5V) .
- Data frequency : 1KHz .
- Digital designs allow the slides to modify and design development for results and better through reprogramming, depending on the user's desire.

Keywords: Digital Modulator **,** ASK , FSK , BPSK , QPSK , DDFS , QDDFS ,FPGA.

I. INTRODUCTION

The mathematical principle of digital modulation using DDFS can be explained according to the diagram [1] shown in figure (1), where the ASK modulation achieved on multiply of data signal and samples of sinusoidal signal [2] stored in ROM , where the data signal , carrier signal and ASK signal shown in figure (2).

FSK modulation achieved on adding frequency code of signal with (0) If data bit equal (0) and adding frequency code of signal with frequency deviation code (DF) [2] when data bit equal (1) so that before the phase accumulator (PA) , where the data signal , carrier signal and FSK signal shown in figure (3).

BPSK modulation achieved on adding phase code of signal with (0) if data bit equal (0) and adding phase code of signal with (2^n /2) for data bit equal (1) so that after (PA) [2] , where the data signal , carrier signal and BPSK signal shown in figure (4).

QPSK modulation achieved on adding (I. cos w t) and (Q. sin w t) signals from the QDDFS , where: I=1 or -1 and Q=1, or -1 , where the data signal , I component , Q component and QPSK signal shown in figure (5) , where the red signal is sine reference signal and blue signal is QPSK signal.

The stored values of the sine and cosine signals in ROM of DDFS and QDDFS are calculated according to the following equation [3]:

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$$U_{SIN}(i) = INT\left[\left(2^{m-1}-1\right).SIN\left(\frac{360.i}{2^b}\right)\right] \quad (1)$$

$$U_{COS}(i) = INT\left[\left(2^{m-1}-1\right).COS\left(\frac{360.i}{2^b}\right)\right]$$

For:

$$\mathrm{m} = 8\,\mathrm{bits}\,,\ \mathrm{b} = 13\,\mathrm{bits}\,,\ i = (0....2^b - 1) = (0...8191)$$

Then:

$$U_{SIN}(i) = INT\left[\left(2^{8-1}-1\right).SIN\left(\frac{360.i}{2^{13}}\right)\right] = INT\left[127.SIN\left(\frac{360.i}{8192}\right)\right]$$

$$U_{COS}(i) = INT\left[\left(2^{8-1}-1\right).COS\left(\frac{360.i}{2^{13}}\right)\right] = INT\left[127.COS\left(\frac{360.i}{8192}\right)\right]$$

$$U_{SIN}(i) = (-127..... +127)$$
$$U_{COS}(i) = (-127..... +127)$$

To avoid negative values that are difficult to store in memory, we add a value off-set= 128

$$U_{SIN}(i) = (0.....255)$$
$$U_{COS}(i) = (0.....255)$$

In paper [4] present the design and simulation only of a modulation module for ASK using VHDL.

In paper [5] present the design and simulation of a modulation module for ASK ,FSK,BPSK,QPSK using VHDL.

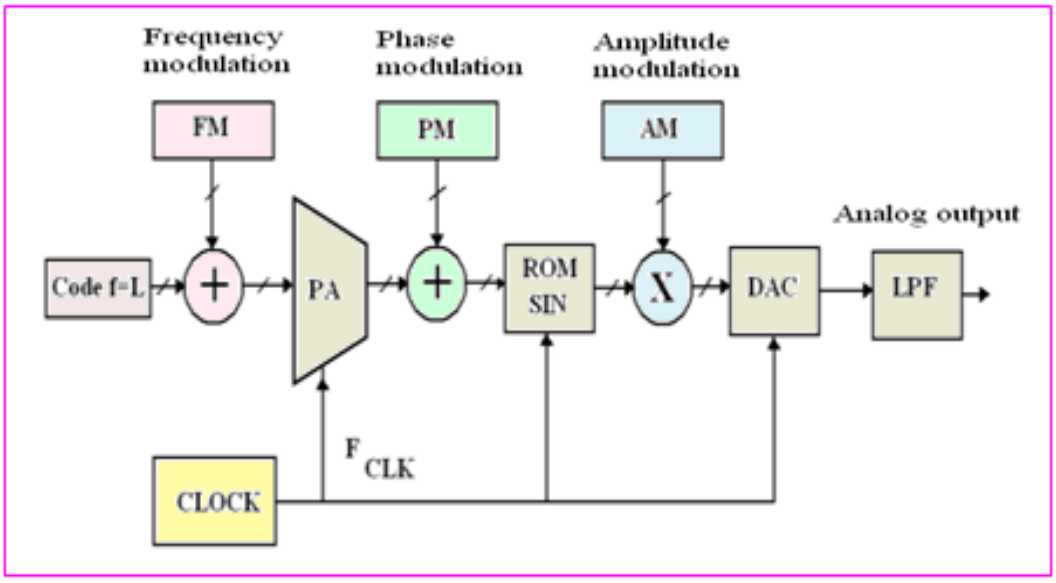

Fig (1) Block diagram of digital modulator using DDFS

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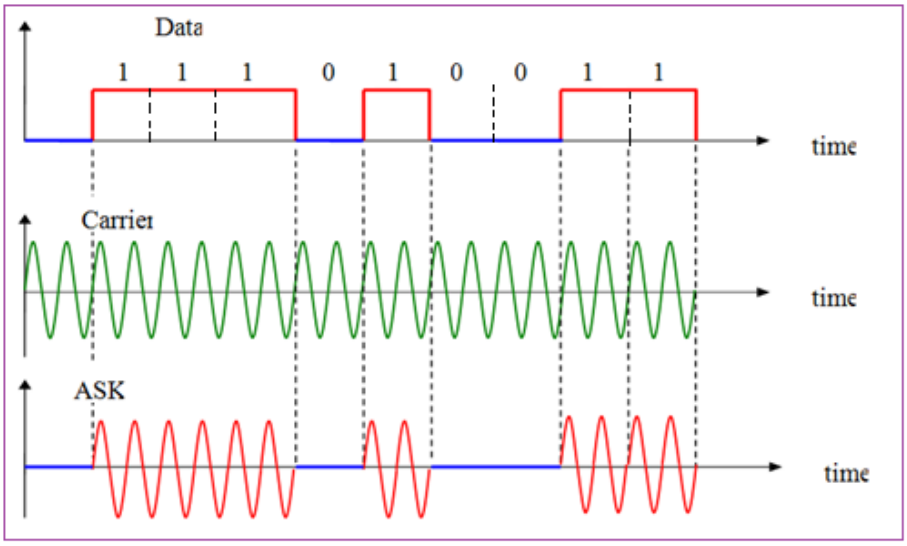

Fig (2) data signal, carrier signal and ASK signal

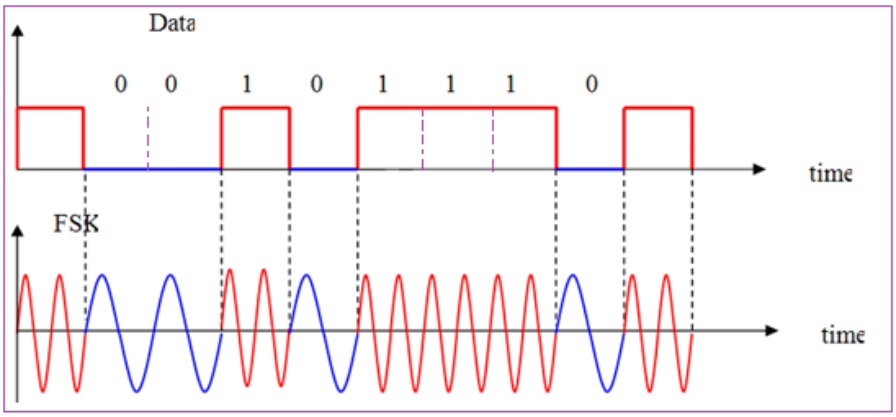

Fig (3) data signal, carrier signal and FSK signal

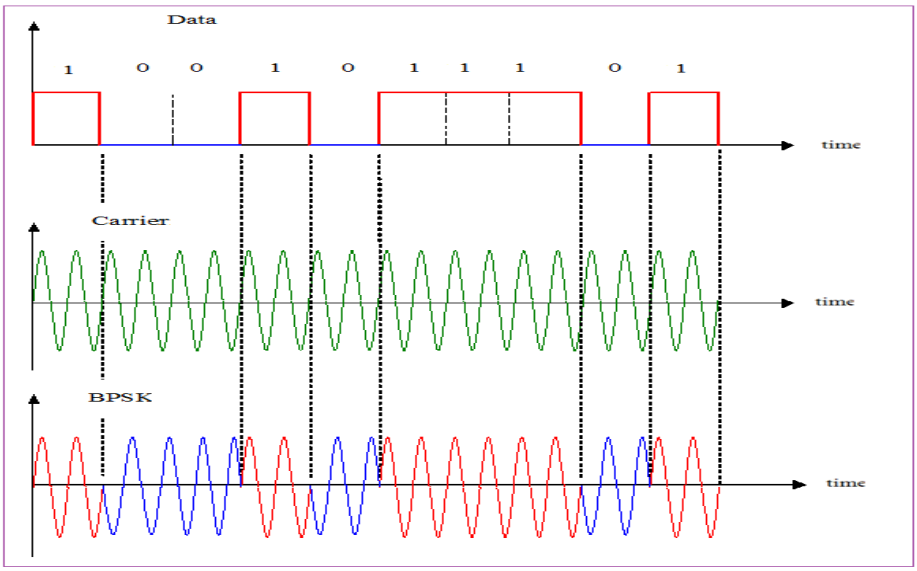

Fig (4) data signal , carrier signal and BPSK signal

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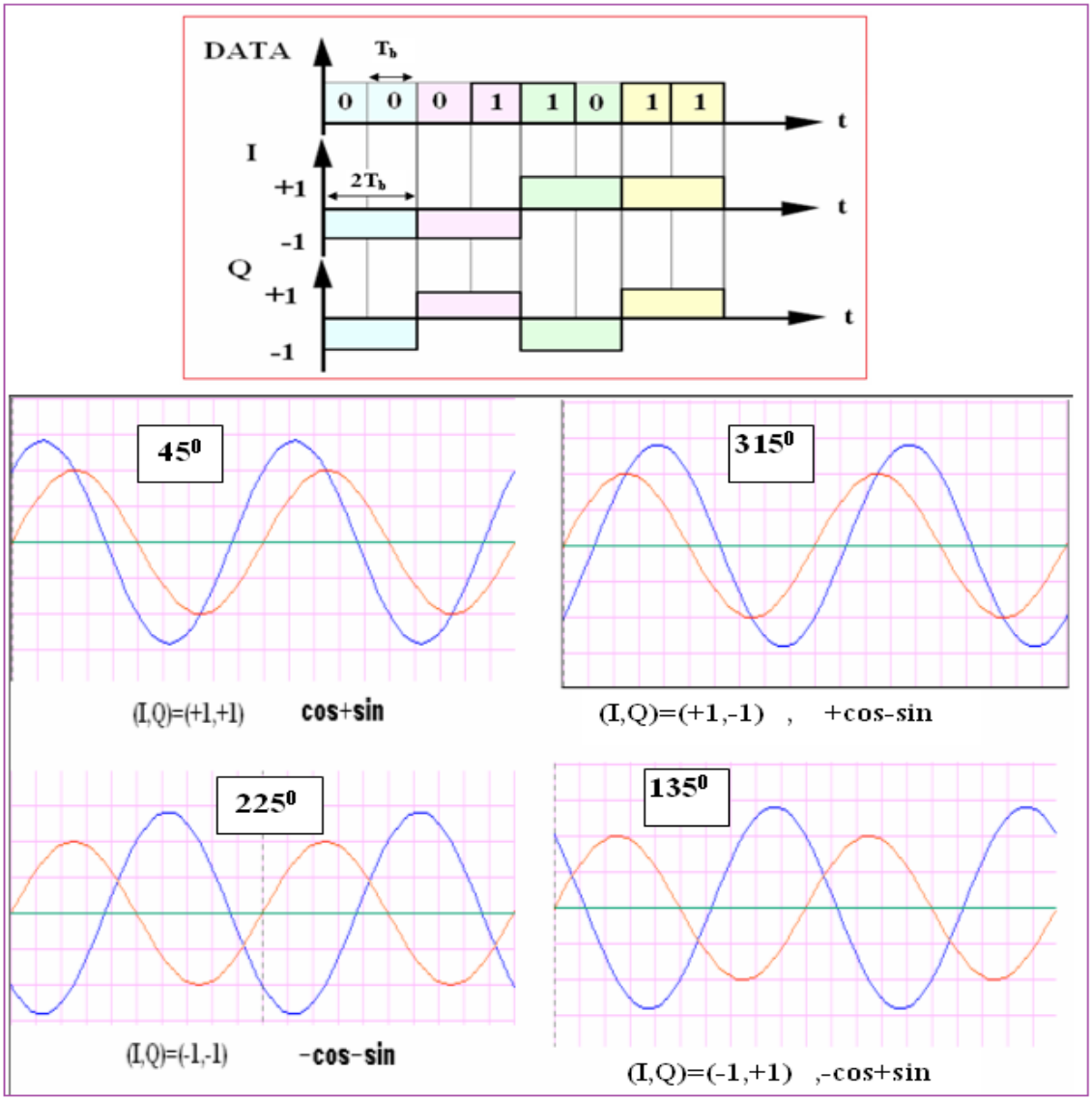

Fig (5) data signal , I, Q ,carrier signal and QPSK signal

II. RESEARCH IMPORTANCE AND ITS OBJECTIVES

-In this paper digital ASK (coherence and non – coherence) ,FSK, BPSK modulators were designed, implemented and tested based on the use of Digital Direct Frequency Synthesizer (DDFS) using FPGA, VHDL and Graphical programming language with Quartus II 9.1 design environment.

-Using the digital DDFS with mathematical operations (adding , multiply , division) , makes the digital modulation design process flexible, accurate and highly efficient.

-Changing the data signal frequency , carrier signal frequency, frequency deviation and phase shift within different values explains the difference between digital modulation and analog modulation .

III. RESEARCH MATERIALS AND ITS WAYS

To design, and test the digital modulators for different modulation types of signals, the following tools and software are used:
-Cyclone II EP2C20F484C7 FPGA chip from ALTERA with highly accuracy, speed, and level specifications, placed on education and development board DE-1 [6].
-DDFS which is considered as highly accuracy techniques in sinusoidal and square signals synthesizing on FPGA chips.

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-VHDL programming language with Quartus II 9.1 design environment [7].
-Design Environment MATLAB R2008a
-GDS-1052 digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the FPGA chip.
The block diagram of the laboratory experiment platform [8] is shown in figure (6).

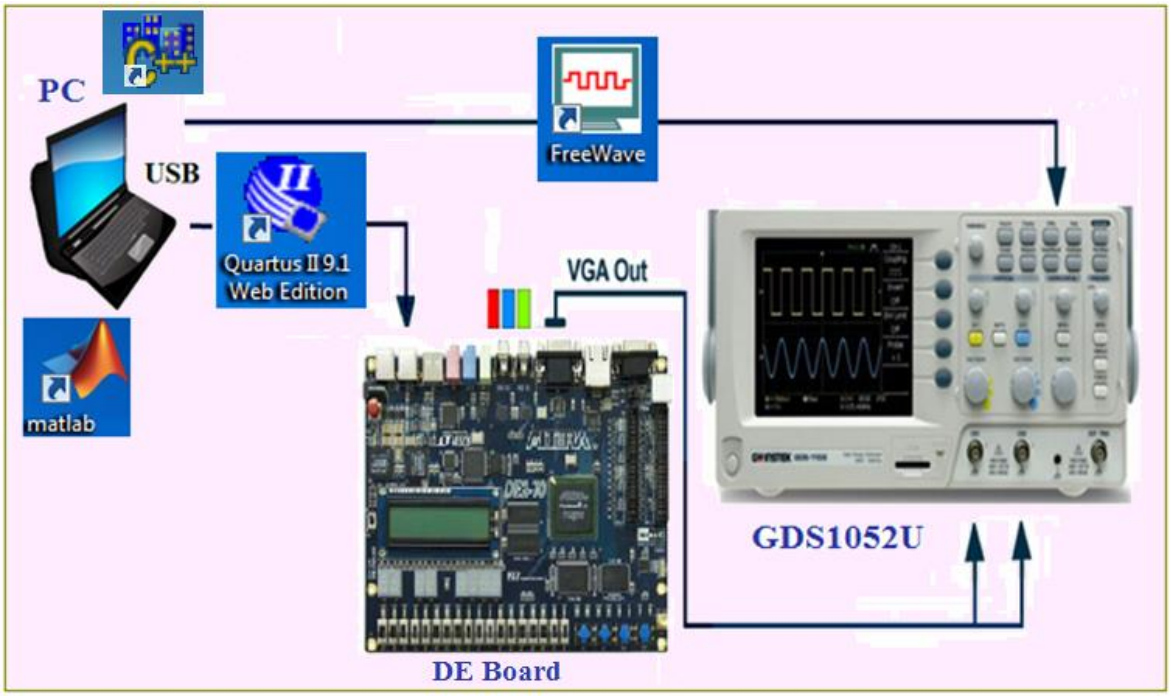

Fig (6) Block diagram of the laboratory experiment platform

IV. BLOCK AND FUNCTIONAL DIAGRAMS OF A DIGITAL ASK MODULATOR

The ASK signal is given according to the fallowing equation [3]:

$$U_{ASK}(t) = \begin{cases} \sin(2\pi ft) & \text{for bit 1} \\ 0 & \text{for bit 0} \end{cases} \qquad (2)$$

The signal frequency and signal frequency code (L) is calculated according to the fallowing equation[3]:

$$f = \frac{L.F_{CLK}}{2^n}$$

$$Code\,\mathrm{f} = L_1 = \frac{f.2^n}{F_{CLK}} \quad , \text{for bit 1} \qquad (3)$$

$$Code\,\mathrm{f} = \mathrm{L}_2 = 0 \quad , \text{for bit 0}$$

The block diagram of digital ASK modulator using DDFS is shown in figure (7) and the functional diagram of digital ASK modulator using DDFS is shown in figure (8).

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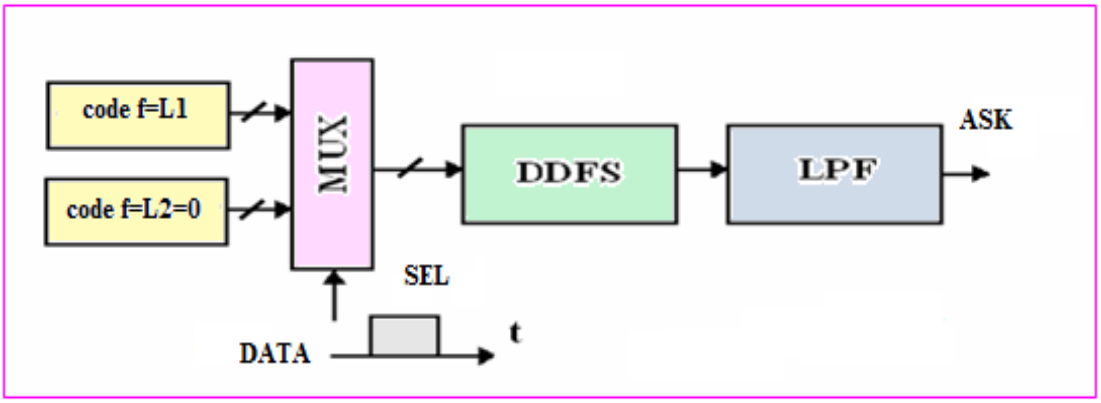

Fig (7) Block diagram of digital ASK modulator using DDFS

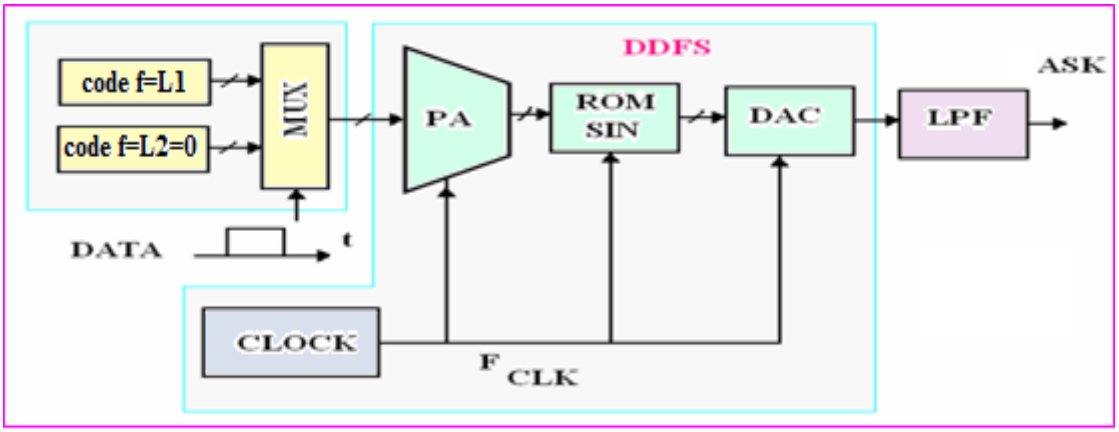

Fig (8) functional diagram of digital ASK modulator using DDFS

The coherence digital ASK modulator is achieved when the initials phase is equal for all radio pulses , it is achieved when data bits (0) reset the phase accumulator, that is very important for radar systems , figure (9).

The functional diagram of coherence digital ASK modulator using DDFS is shown in figure (9).

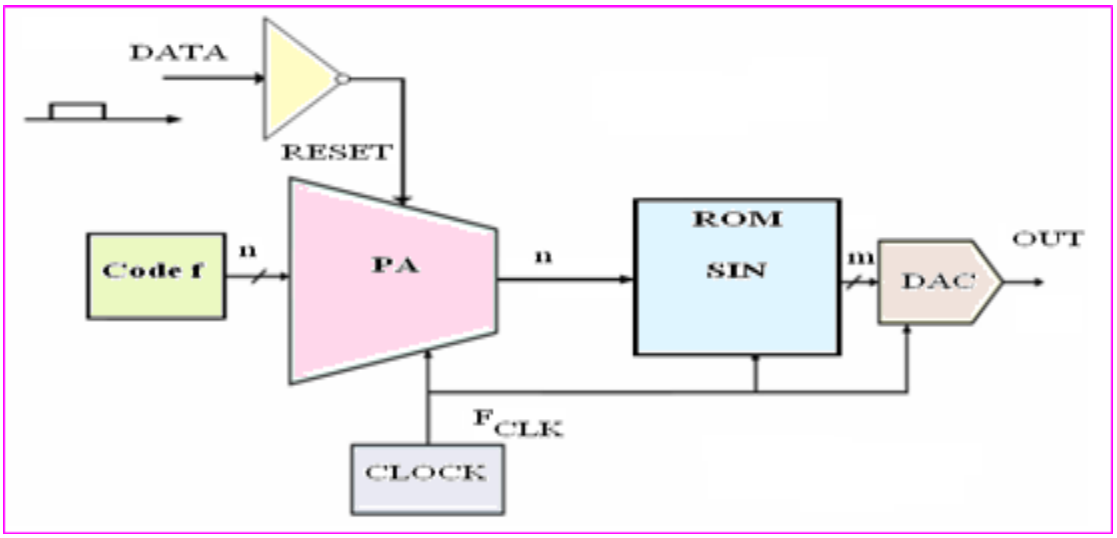

Fig (9) functional diagram of coherence digital ASK modulator using DDFS

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The non -coherence digital ASK , is done when the initials phase of ASK signals is deferent from each other for all bits (1) , it is achieved when data bits (1) passed the values of phase accumulator to ROM DDFS, where the phase of carrier is continued , figure (10).

The functional diagram of non - coherence digital ASK modulator using DDFS is shown in figure (10).

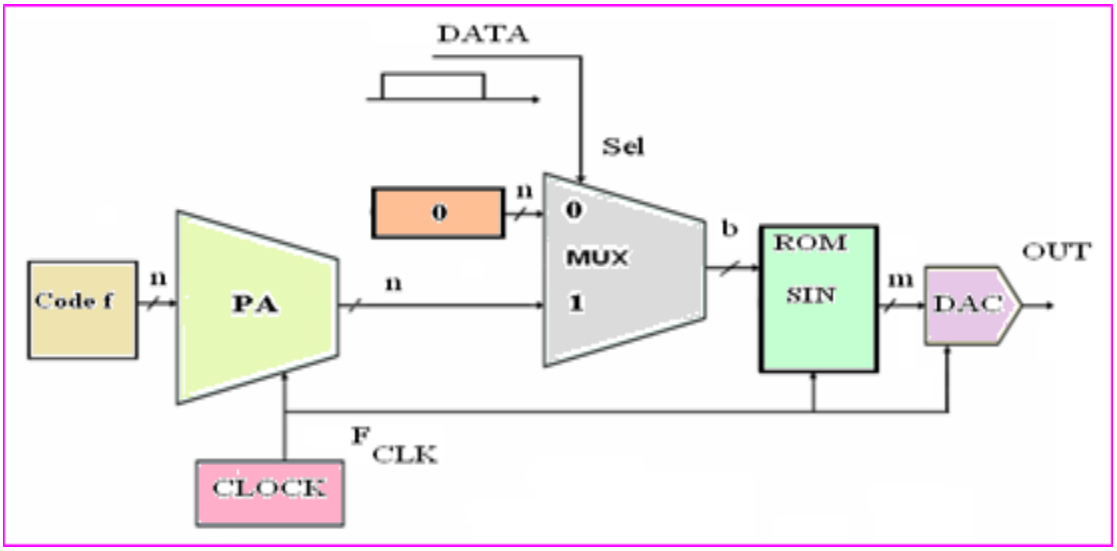

Fig (10) functional diagram of non-coherence digital ASK modulator using DDFS

The functional diagram of coherence digital ASK modulator in Quartus II 9.1 design environment is shown in figure (11), where output signal is data signal, and coherent ASK signals are with the following parameters **[9] :**
-Clock frequency: F_{CLK}=50 MHz.
-Modulation type of signal is : coherence ASK .
-Carrier frequency of ASK: 1 MHz .
-Frequency of data signal: 1 KHz.
-Frequency range: (0.011 Hz…25 MHz).
-Frequency Resolution: (0.011 Hz).
-Size of DDFS ROM: 13KB.
-DAC : with 8 bits.
-Bits numbers of Phase Accumulator : n=32 bits
-Signal amplitude (5V).

$$\delta f = \frac{F_{CLK}}{2^n} \Rightarrow 2^n = \frac{F_{CLK}}{\delta f} = \frac{50*10^6}{0.011} \Rightarrow n = 32 \text{ bits}$$

$$\Delta f = 0.... \frac{F_{CLK}}{2} = 0....25MHz$$

$$F_{OUT} = \frac{F_{CLK}.\ L_1}{2^n}$$

$$CODE\ \text{f} = L_1 = \frac{F_{OUT}.2^n}{F_{CLK}} = \frac{1*2^{32}}{50} = 85899346$$

$$CODE\ 0 = \text{L}_2 = 0$$

$$F_{DATA} = \frac{F_{CLK}.L_{DATA}}{2^n} \Rightarrow L_{DATA} = \frac{2^n.F_{DATA}}{F_{CLK}} = \frac{2^{32}.1}{50.10^3} = 85899$$

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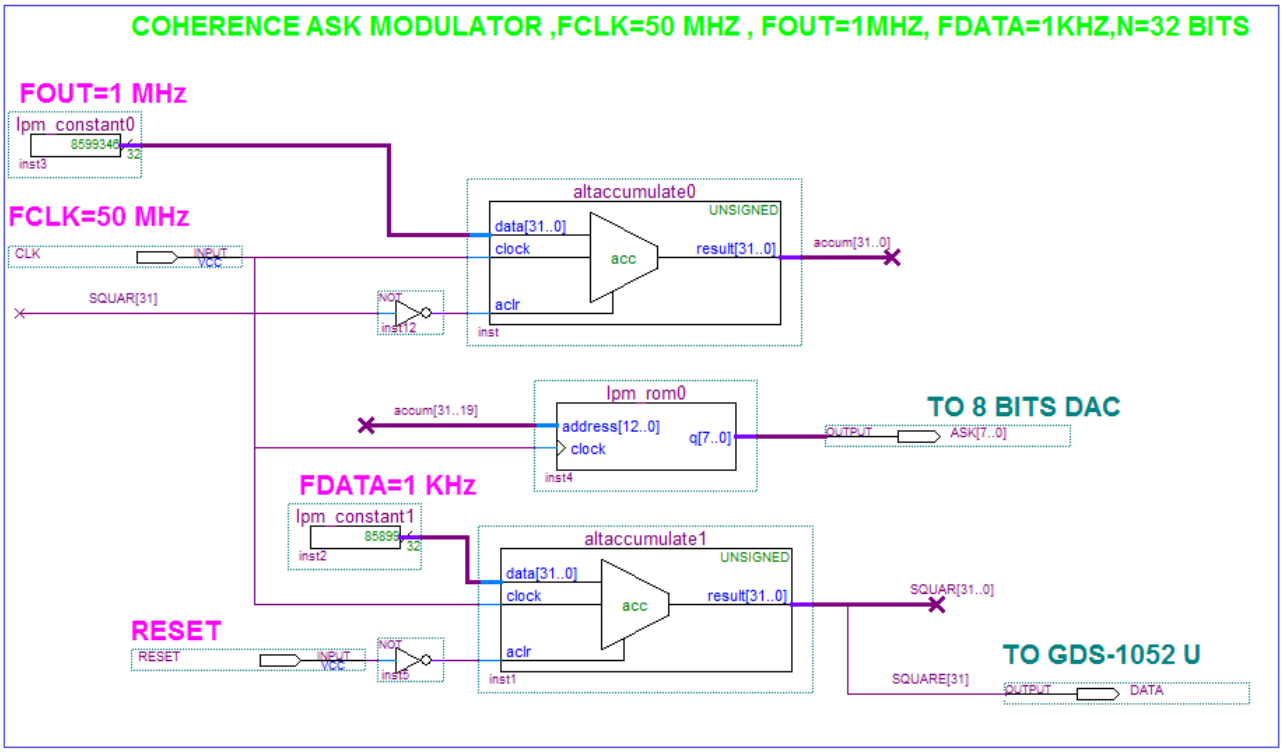

Fig (11) functional diagram of coherent digital ASK modulator in Quartus II 9.1 design environment

The result of designed coherent digital ASK modulator in Quartus II 9.1 design environment is shown in figure (12) in time and frequency domains , where frequency of data signal: 1 KHz , carrier frequency of ASK: 1 MHz .

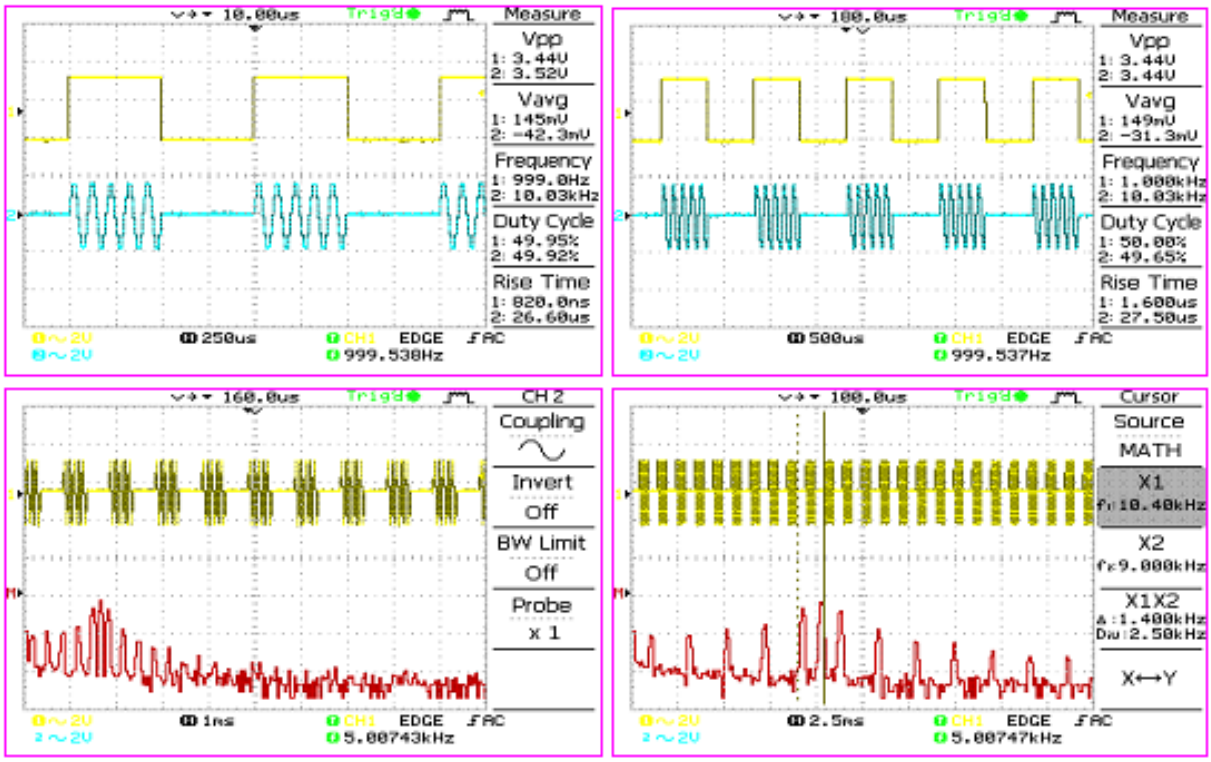

Fig (12) coherent ASK signal in time and frequency domains

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The functional diagram of non -coherent digital ASK modulator in Quartus II 9.1 design environment is shown in figure (13) where output signals are data signal and non -coherent ASK signals **[**9**]**.

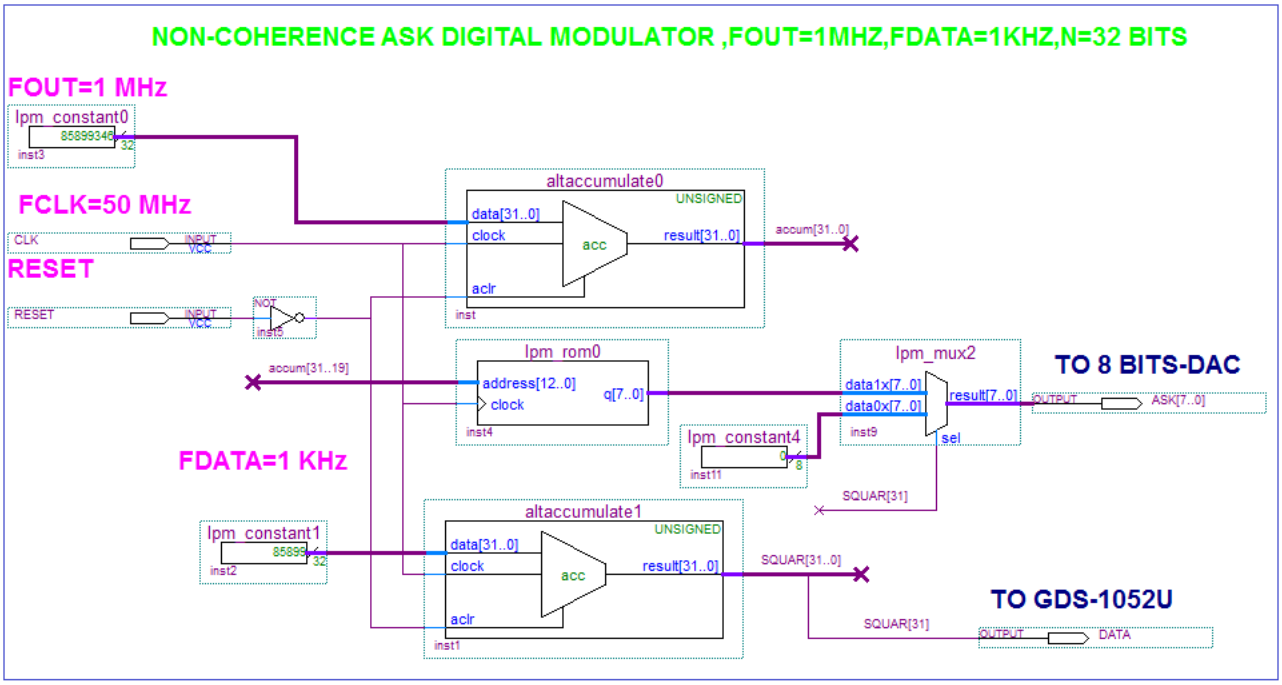

Fig (13) functional diagram of non-coherent digital ASK modulator in Quartus II 9.1 design environment

The result of designed non -coherent digital ASK modulator in Quartus II 9.1 design environment is shown in figure (14) in time domain , where frequency of data signal: 1 KHz , carrier frequency of ASK: 1 MHz .

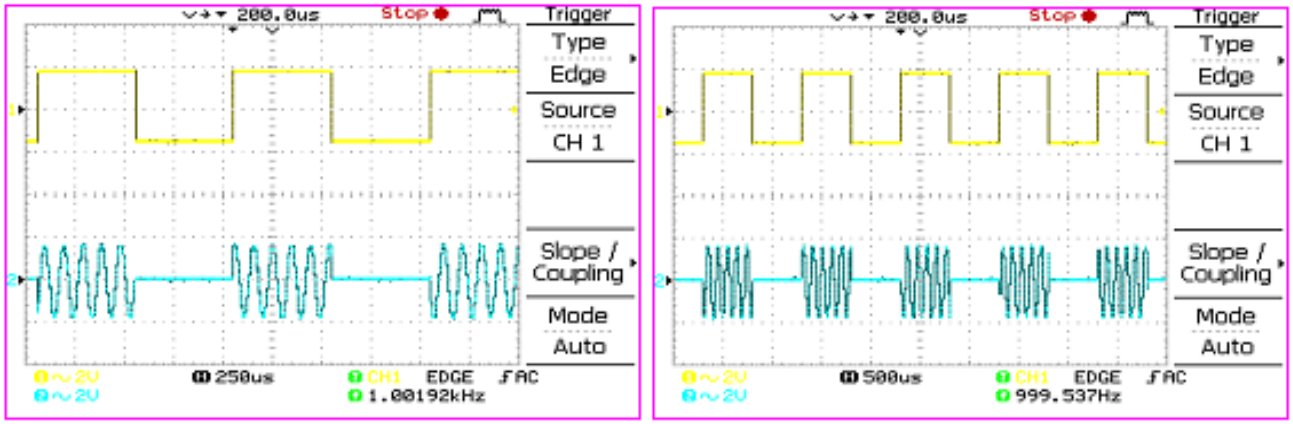

Fig (14) non-coherence ASK signal in time domain

V. BLOCK AND FUNCTIONAL DIAGRAMS OF A DIGITAL FSK MODULATOR

The FSK signal is given according to the fallowing equation [3]

$$U_{FSK}(t) = \begin{cases} \sin(2\pi f_1 t) & \text{for bit } 0 \\ \sin(2\pi f_2 t) & \text{for bit } 1 \end{cases} \quad (4)$$

$$f_2 = f_1 + Df \Rightarrow Df = f_2 - f_1$$

The signal frequency and frequency code (L) is calculated according to the fallowing equation[]

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$$f = \frac{L.F_{CLK}}{2^n}$$

$$CODE\ \mathrm{f}_1 = L_1 = \frac{f_1.2^n}{F_{CLK}}$$

$$CODE\ \mathrm{f}_2 = L_2 = \frac{f_2.2^n}{F_{CLK}} \qquad (5)$$

$$\mathrm{CODE\ Df} = \mathrm{L}_0 = \frac{Df.2^n}{F_{CLK}}$$

The block diagram of digital FSK modulator using DDFS is shown in figure (15) and the functional diagram of digital FSK modulator using DDFS is shown in figure (16).

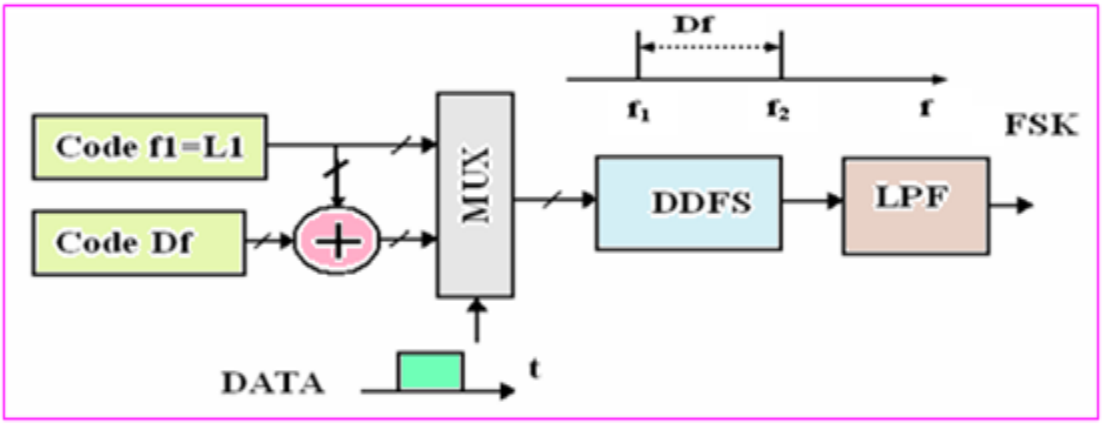

Fig (15) Block diagram of digital FSK modulator using DDFS

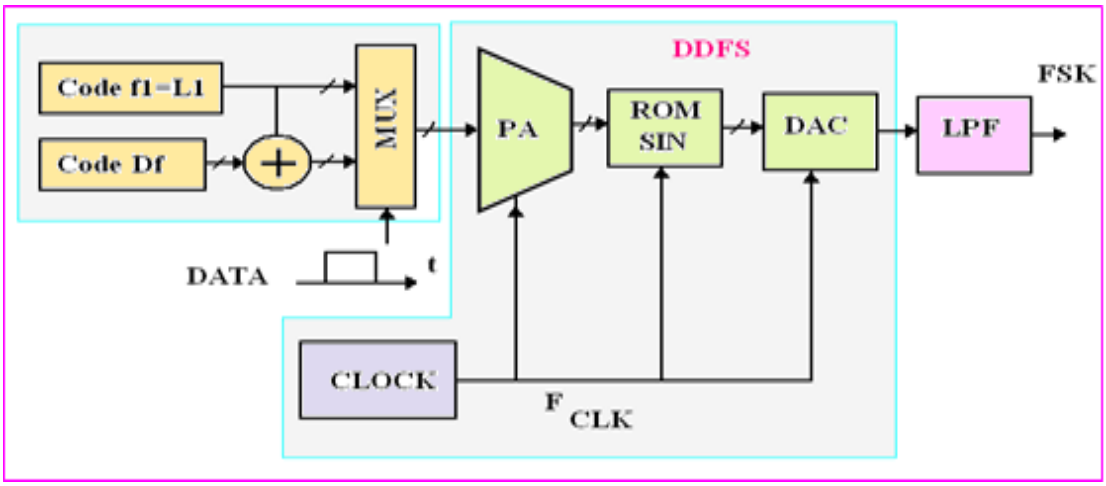

Fig (16) functional diagram of digital FSK modulator using DDFS

The functional diagram of digital FSK modulator in Quartus II 9.1 design environment is shown in figure (17) , where output signals are data signal and FSK signals with the following parameters **[9]:**

-Clock frequency: F_{CLK}=50 MHz
-Modulation type of signal is : FSK.
-Carrier frequency of FSK: f_1= 1 MHz, f_2= 1.025 MHz,
- Frequency deviation of FSK is : DF=25KHz.
-Frequency of data signal: 1 KHz

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-Frequency range: (0.011 Hz…25 MHz).
-Frequency Resolution: (0.011 Hz).
-Size of DDFS ROM: 13KB.
-DAC :with 8 bits.
-Bits numbers of Phase Accumulator : n=32 bits
-Signal amplitude (5V).

$$CODE\ \mathrm{f}_1 = L_1 = \frac{f_1.2^n}{F_{CLK}} = \frac{1*2^{32}}{50} = 85899346$$

$$CODE\ \mathrm{f}_2 = \mathrm{L}_2 = \frac{f_2.2^n}{F_{CLK}} = \frac{1.025*2^{32}}{50} = 88046830$$

$$CODE\ \mathrm{Df} = \mathrm{L}_0 = \frac{Df.2^n}{F_{CLK}} = \frac{0.025*2^{32}}{50} = 2147484$$

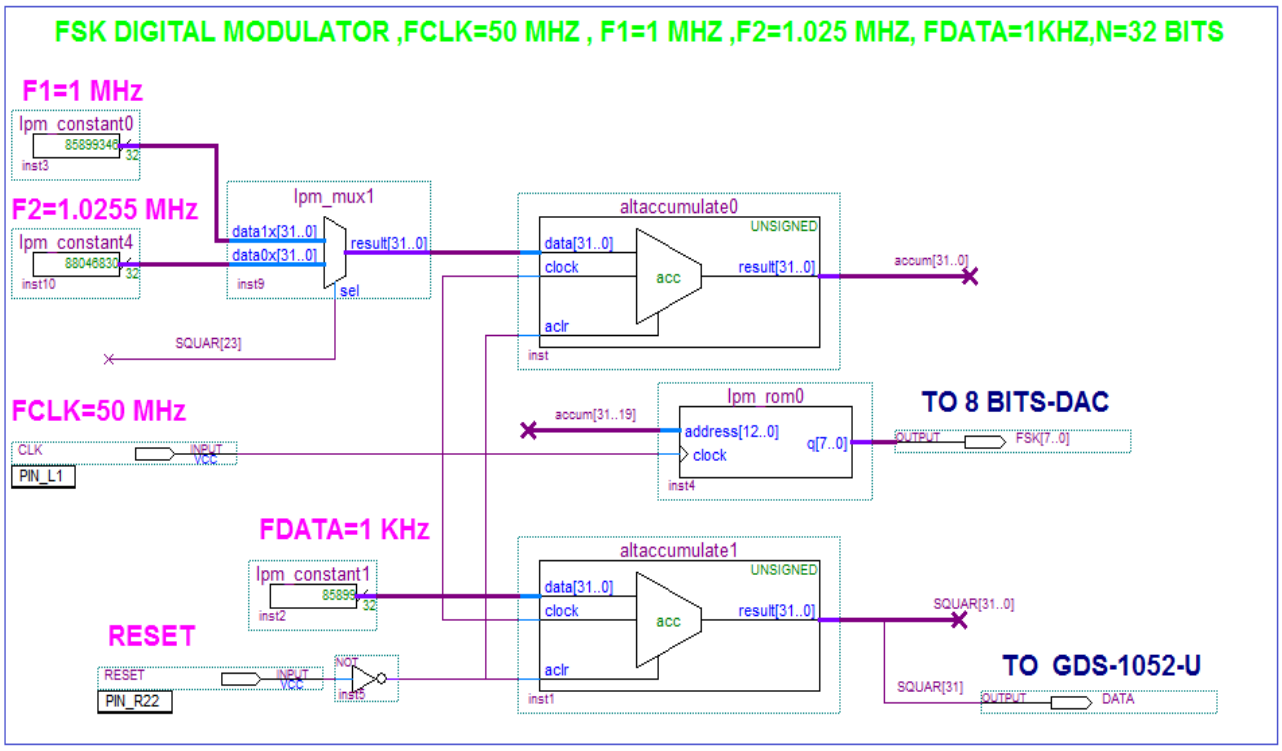

Fig (17) functional diagram of digital FSK modulator in Quartus II 9.1 design environment

The result of designed digital FSK modulator in Quartus II 9.1 design environment is shown in figure (18) in time and frequency domains , where frequency of data signal: 1 KHz , carrier frequency of FSK: 1 MHz , deviation frequency : 25 KHz.

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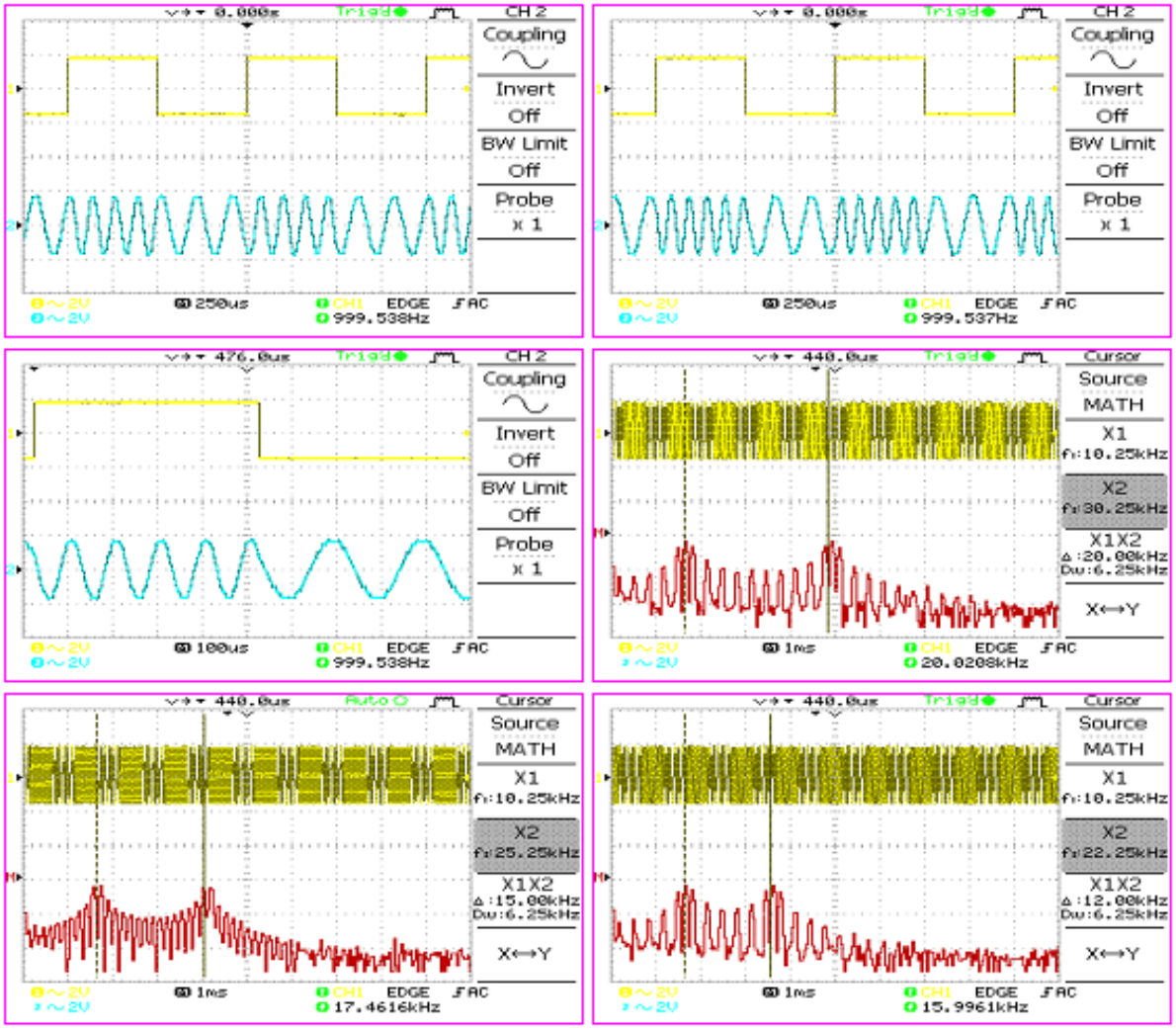

Fig (18) FSK signal in time and frequency domains

VI. BLOCK AND FUNCTIONAL DIAGRAMS OF A DIGITAL BPSK MODULATOR

The BPSK signal is given according to the fallowing equation [3]

$$U_{BPSK}(t) = \begin{cases} \sin(2\pi\ f\ t) & \text{for bit 1} \\ \sin(2\pi\ f\ t + \pi) & \text{for bit 0} \end{cases} \qquad (6)$$

The signal frequency ,frequency code (L) and phase code are calculated according to the fallowing equations [3]

$$f = \frac{L.F_{CLK}}{2^n}$$

$$CODE\ \mathrm{f} = L = \frac{2^n.f}{F_{CLK}} \qquad (7)$$

$$\text{PHASE CODE}\ (0) = \mathrm{X}_{\varphi 0} = 0$$

$$\text{PHASE CODE}\ (\pi) = \mathrm{X}_{\varphi 1} = \frac{2^n.\pi}{2\pi} = \frac{2^n}{2} \qquad (8)$$

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DATA	0	1
PHASE	π	0
PHASE CODE	$X_{\varphi 1} = \frac{2^n.\pi}{2\pi} = \frac{2^n}{2}$	$X_{\varphi 0} = \frac{2^n.0}{2\pi} = 0$

The block diagram of digital BPSK modulator using DDFS is shown in figure (19), and the functional diagram of digital BPSK modulator using DDFS is shown in figure (20).

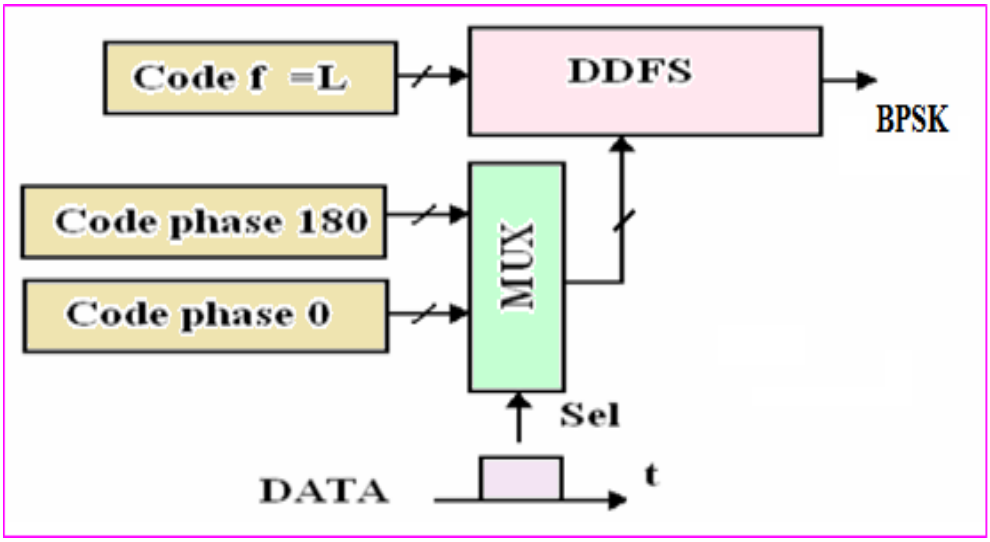

Fig (19) Block diagram of digital BPSK modulator using DDFS

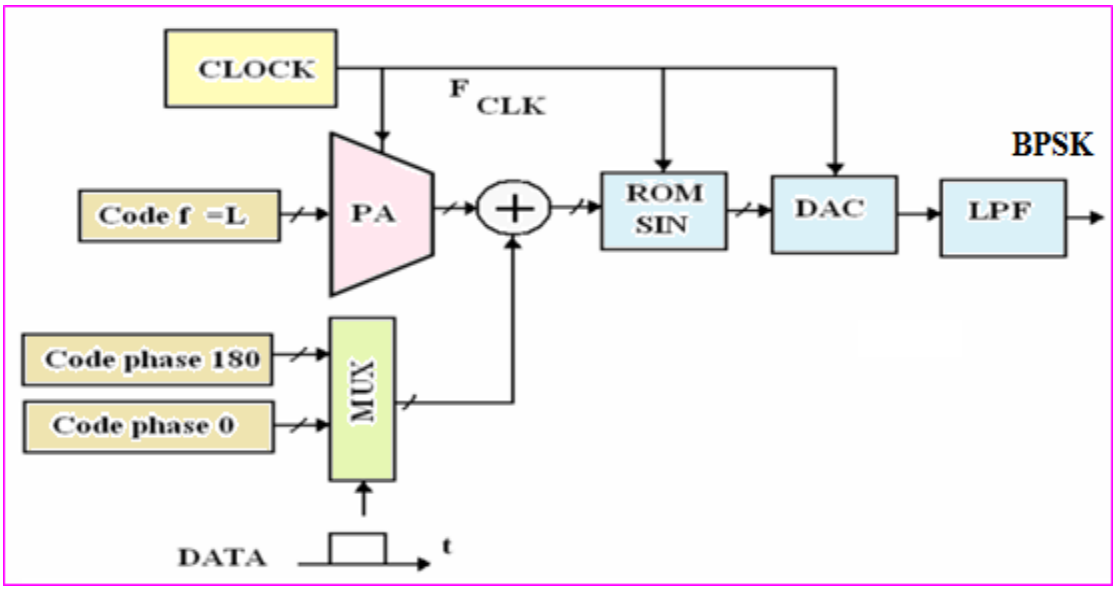

Fig (20) functional diagram of digital BPSK modulator using DDFS

The functional diagram of digital BPSK modulator in Quartus II 9.1 design environment is shown in figure (21) where output signals are data signal and BPSK signals with the following parameters **[**9**]:**

-Clock frequency: F_{CLK}=50 MHz
-Modulation type of signal is : BPSK.
-Carrier frequency of BPSK: f= 1 MHz.
- PHASE SHIFT of BPSK is : 180^0.
-Frequency of data signal: 1 KHz
-Frequency range: (0.011 Hz…25 MHz).

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-Frequency Resolution: (0.011 Hz).
-Size of DDFS ROM: 13KB.
-DAC :with 8 bits.
-Bits numbers of Phase Accumulator : n=32 bits
-Signal amplitude (5V).

$$CODE\ f_1 = L_1 = \frac{f.2^n}{F_{CLK}} = \frac{1*2^{32}}{50} = 85899346$$

$$\text{PHASE CODE } (0) = X_{\varphi 0} = \frac{2^n.0}{2\pi} = 0$$

$$\text{PHASE CODE } (\pi) = X_{\varphi 1} = \frac{2^n.\pi}{2\pi} = \frac{2^n}{2} = \frac{2^{32}}{2} = 2147483648$$

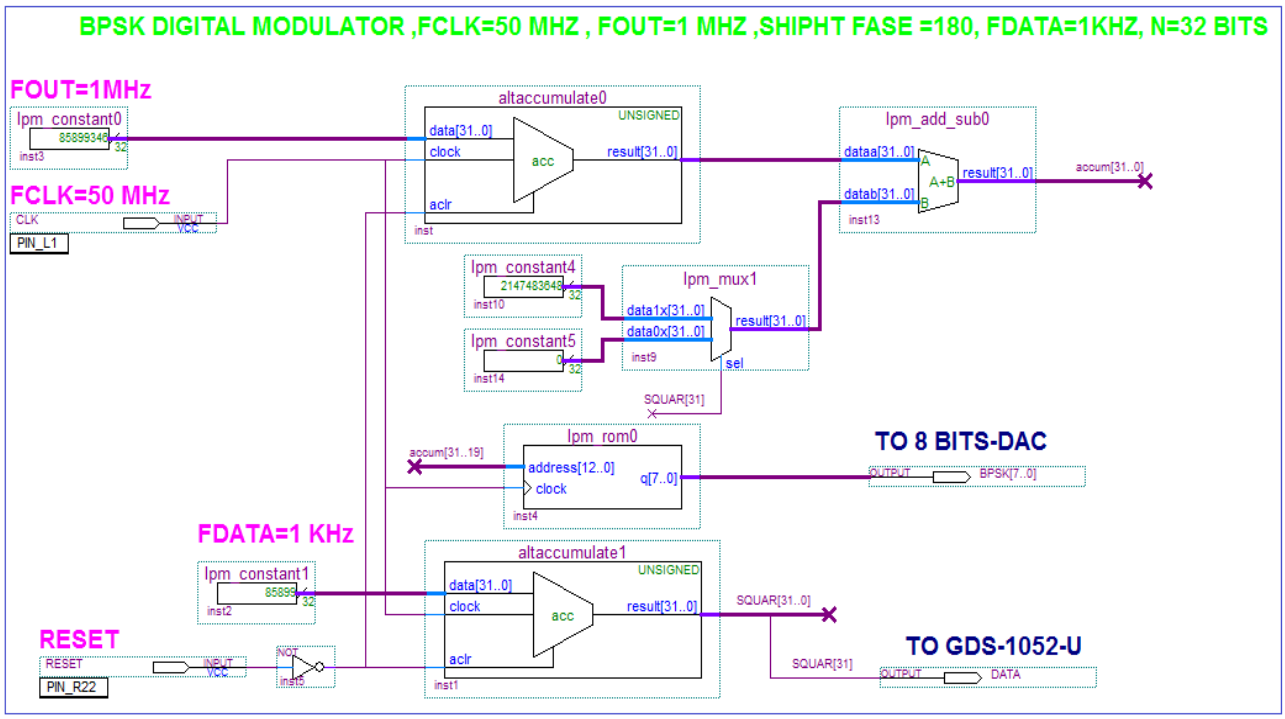

Fig (21) functional diagram of digital BPSK modulator in Quartus II 9.1 design environment

The result of designed digital BPSK modulator in Quartus II 9.1 design environment is shown in figure (22) in time and frequency domains , where frequency of data signal: 1 KHz , carrier frequency of BPSK: 1 MHz , phase shift: 180^0.

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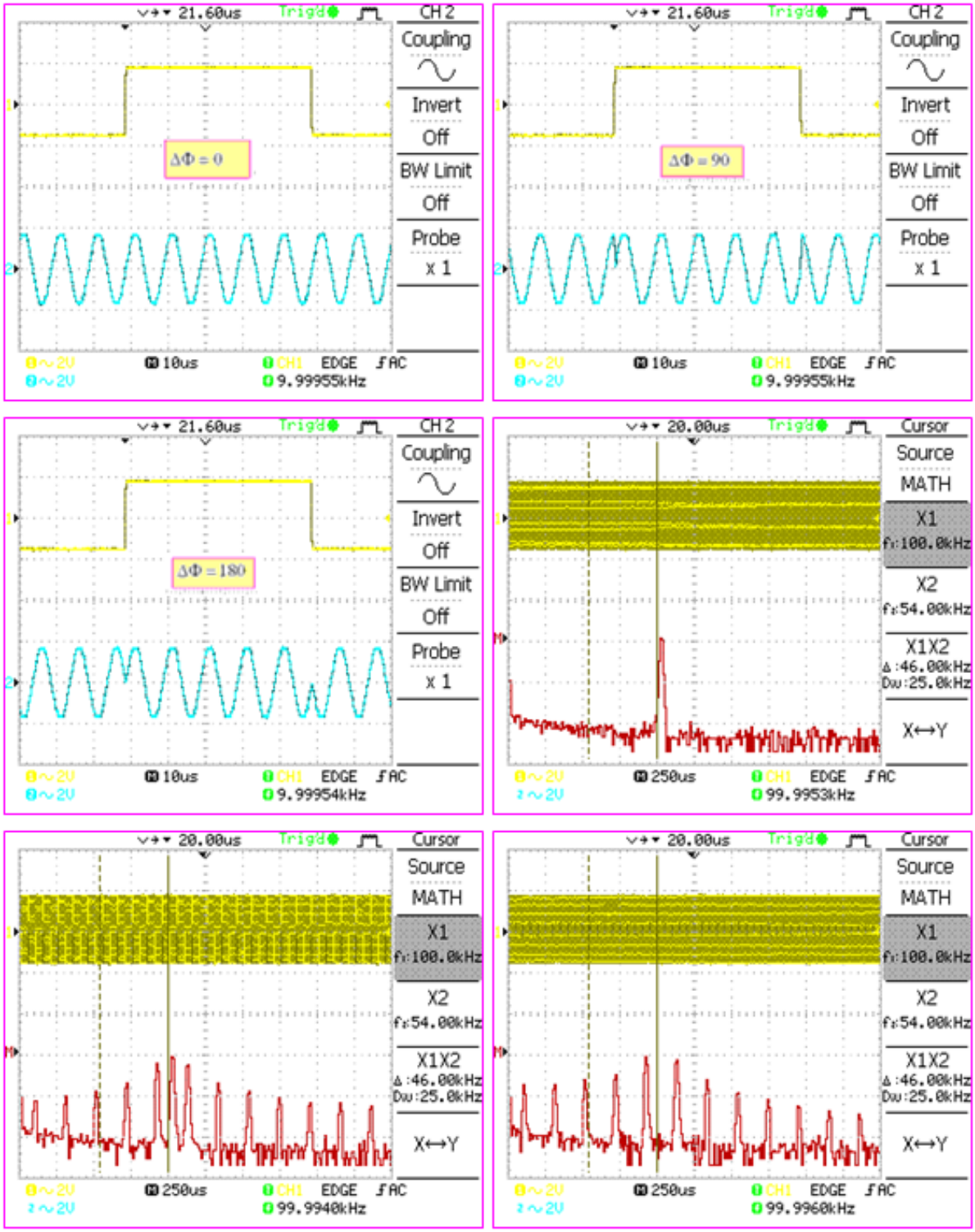

Fig (22) BPSK signal in time and frequency domains

VII. BLOCK AND FUNCTIONAL DIAGRAMS OF A DIGITAL QPSK MODULATOR

The QPSK signal is given according to the fallowing equation [3] , values of Data , I component, Q component and phase of QPSK given according to the table .1 and figure (23).

$$U_{QPSK}(t) = \mathrm{I}.\cos(2\pi\ f\ t) + \mathrm{Q}.\sin(2\pi\ f\ t) \quad , \mathrm{I} = +1 \text{ or } -1 \text{ and } \mathrm{Q} = +1 \text{ or } -1 \qquad (9)$$

Table.1 values of Data , I , Q , Out QPSK and phase of QPSK

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Data	I	Q	I.cos	Q.sin	Out (QPSK)	Phase
00	-1	-1	-cos	-sin	- cos – sin	225^0
01	-1	+1	- cos	+ sin	- cos + sin	135^0
10	+1	-1	+ cos	- sin	+ cos – sin	315^0
11	+1	+1	+ cos	+ sin	+ cos + sin	45^0

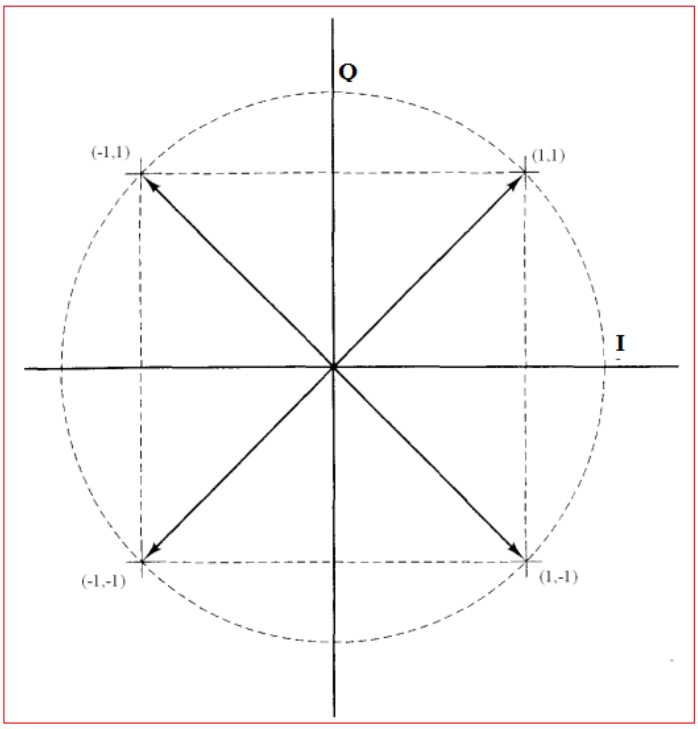

Fig (23) values of Data , I , Q and phase of QPSK

The signal frequency ,frequency code (L) is calculated according to the fallowing equations [3]

$$f = \frac{L.F_{CLK}}{2^n} \qquad (10)$$

The block diagram of digital QPSK modulator using QDDFS is shown in figure (24), and the functional diagram of digital QPSK modulator using QDDFS is shown in figure (25).

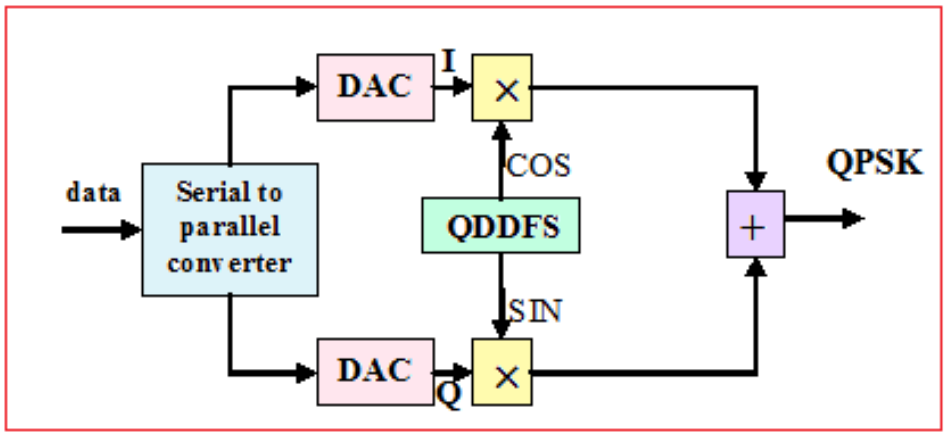

Fig (24) Block diagram of digital QPSK modulator using QDDFS

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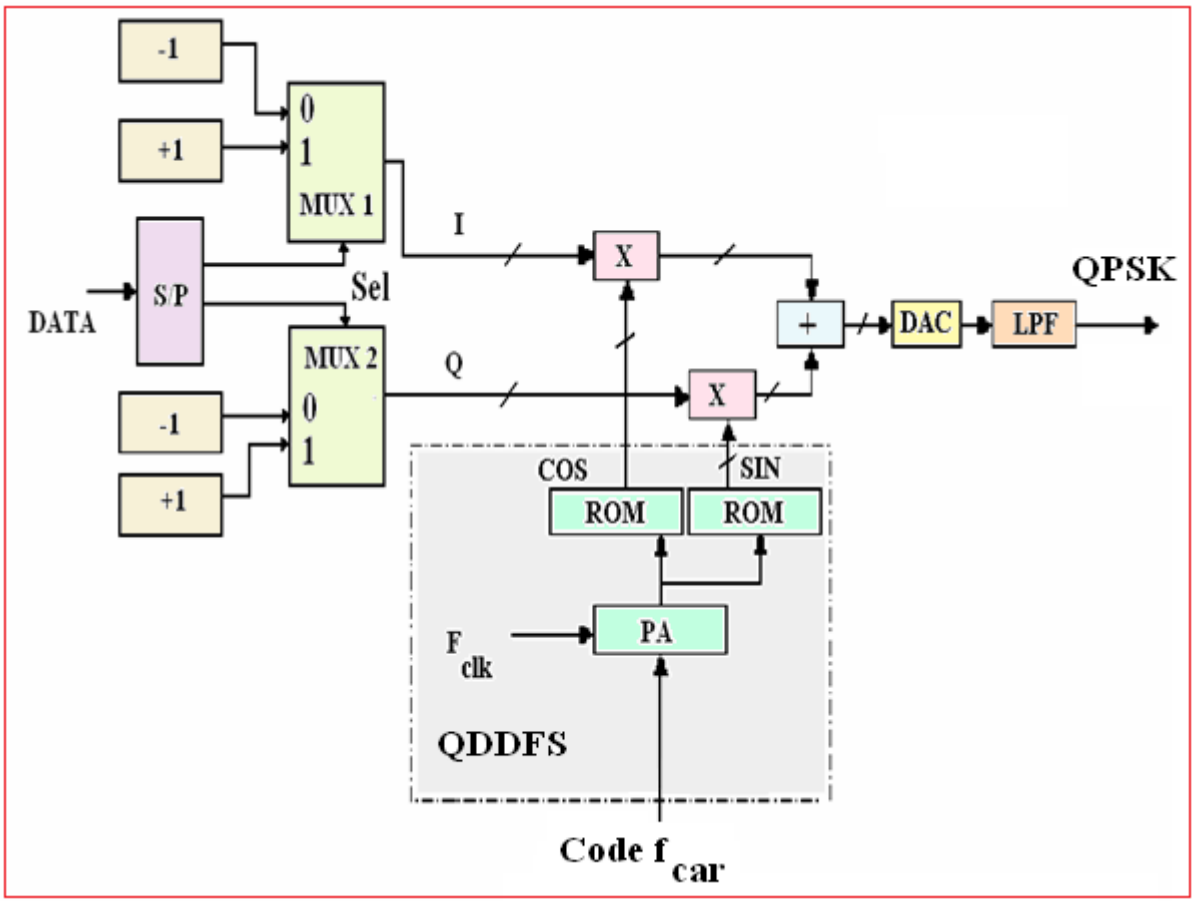

Fig (25) functional diagram of digital QPSK modulator using QDDFS

The functional diagram of digital QPSK modulator in Quartus II 9.1 design environment is shown in figure (26) where output signals are data signal and QPSK signal with the following parameters **[9]:**

-Clock frequency: F_{CLK}=50 MHz
-Modulation type of signal is : QPSK.
-Carrier frequency of QPSK : f= 1 MHz.
- PHASE SHIFT of QPSK is : 45^0 , 135^0 , 225^0, 315^0 .
-Frequency of data signal: 1 KHz
-Frequency range of QDDFS: (0.011 Hz…25 MHz).
-Frequency Resolution of QDDFS : (0.011 Hz).
-Size of QDDFS ROM: 2 x 13KB.
-DAC :with 8 bits.
-Bits numbers of Phase Accumulator : n=32 bits
-Signal amplitude (5V).

$$CODE\ f_1 = L_1 = \frac{f.2^n}{F_{CLK}} = \frac{1*2^{32}}{50} = 85899346$$

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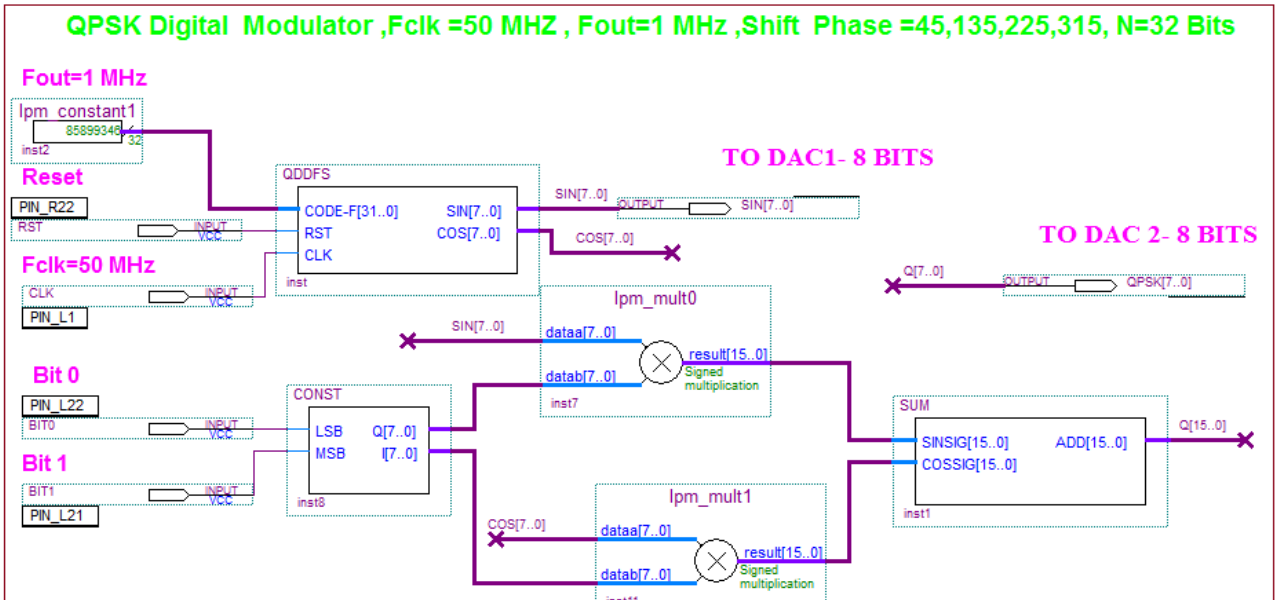

Fig (26) functional diagram of digital QPSK modulator in Quartus II 9.1 design environment

The result of designed digital QPSK modulator in Quartus II 9.1 design environment is shown in figure (27) in time domains and is shown in figure (28) in frequency domains , where frequency of data signal : 1 KHz , carrier frequency of QPSK: 1 MHz , phase shift : 45^0 , 135^0 , 225^0, 315^0.

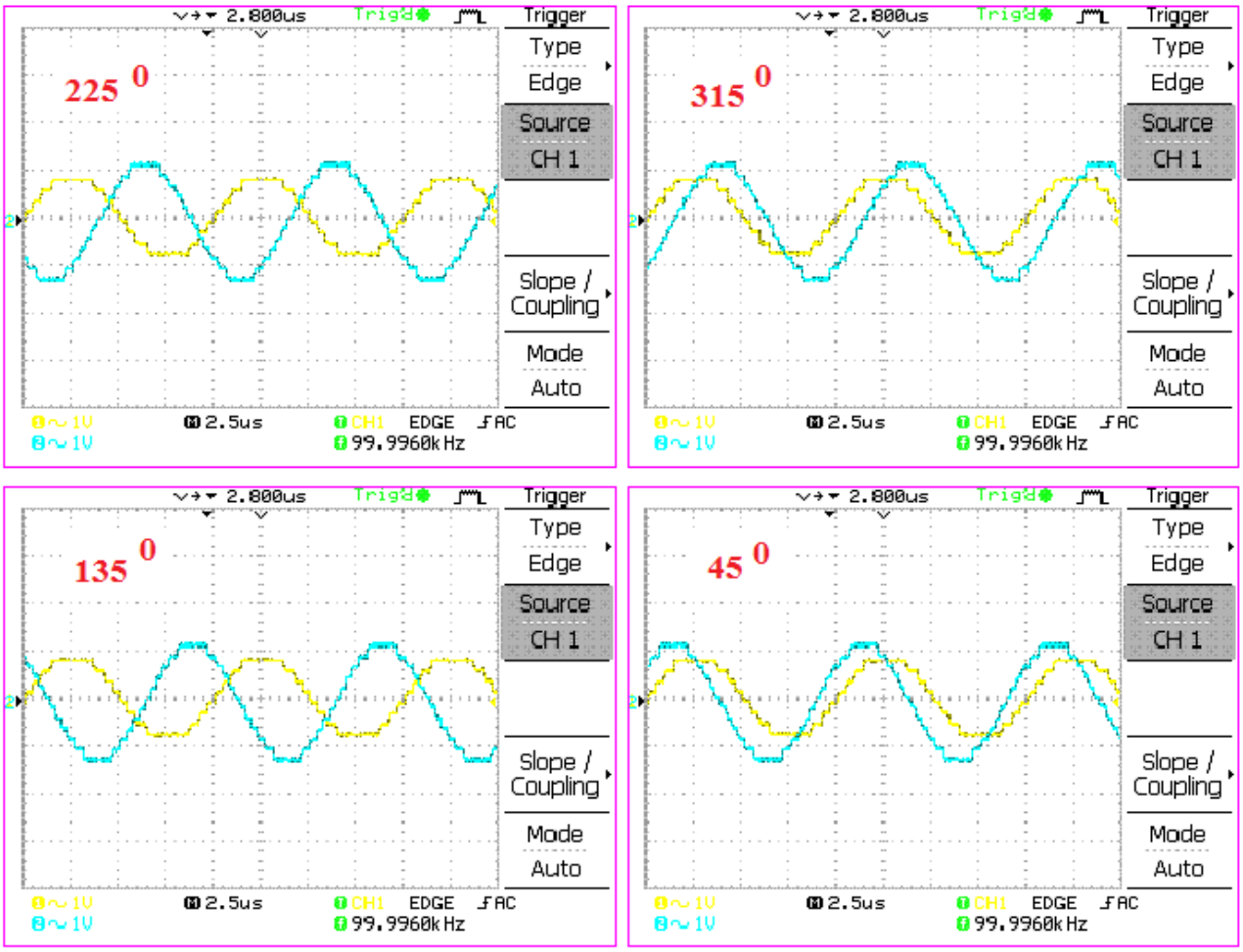

Fig (27) QPSK signal in time domain for shift phase : 45^0 , 135^0 , 225^0, 315^0

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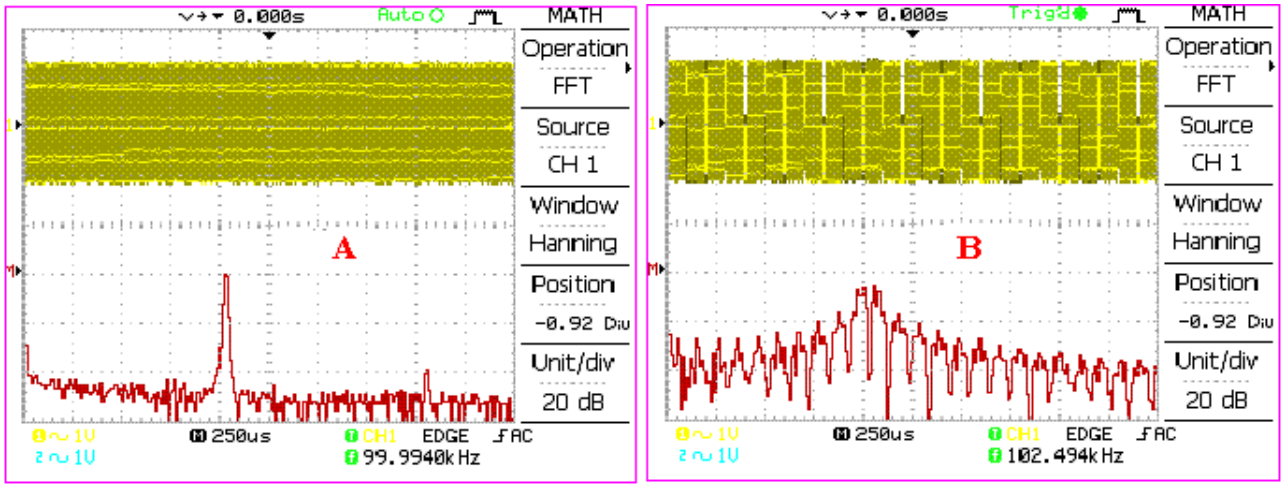

Fig (28) carrier (A) and QPSK (B) signals in frequency domains

VIII. DISCUSSION AND CONCLUSION

-Depending on the previous practical results ,the digital ASK ,FSK , BPSK and QPSK modulators were successfully designed using FPGA.
- In this research, the digital modulators were designed with-DDFS and QDDFS which is considered as a highly accuracy technique in carrier sinusoidal , data signal, and ASK,FSK,BPSK and QPSK synthesizing on FPGA chips.
- Practical experiments described in the study suggest how these modulators can be used in real communication devices.
- There is a possibility to develop this algorithm through designing digital QAM-16, QAM-32 and QAM-64 and another modulators types.

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